F9J SCHEMATIC Revision 2.0

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<Variant Name>

ASUSTeK COMPUTER INC

Title : PAGE REF.

Engineer:

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Custom	F9J	2.0

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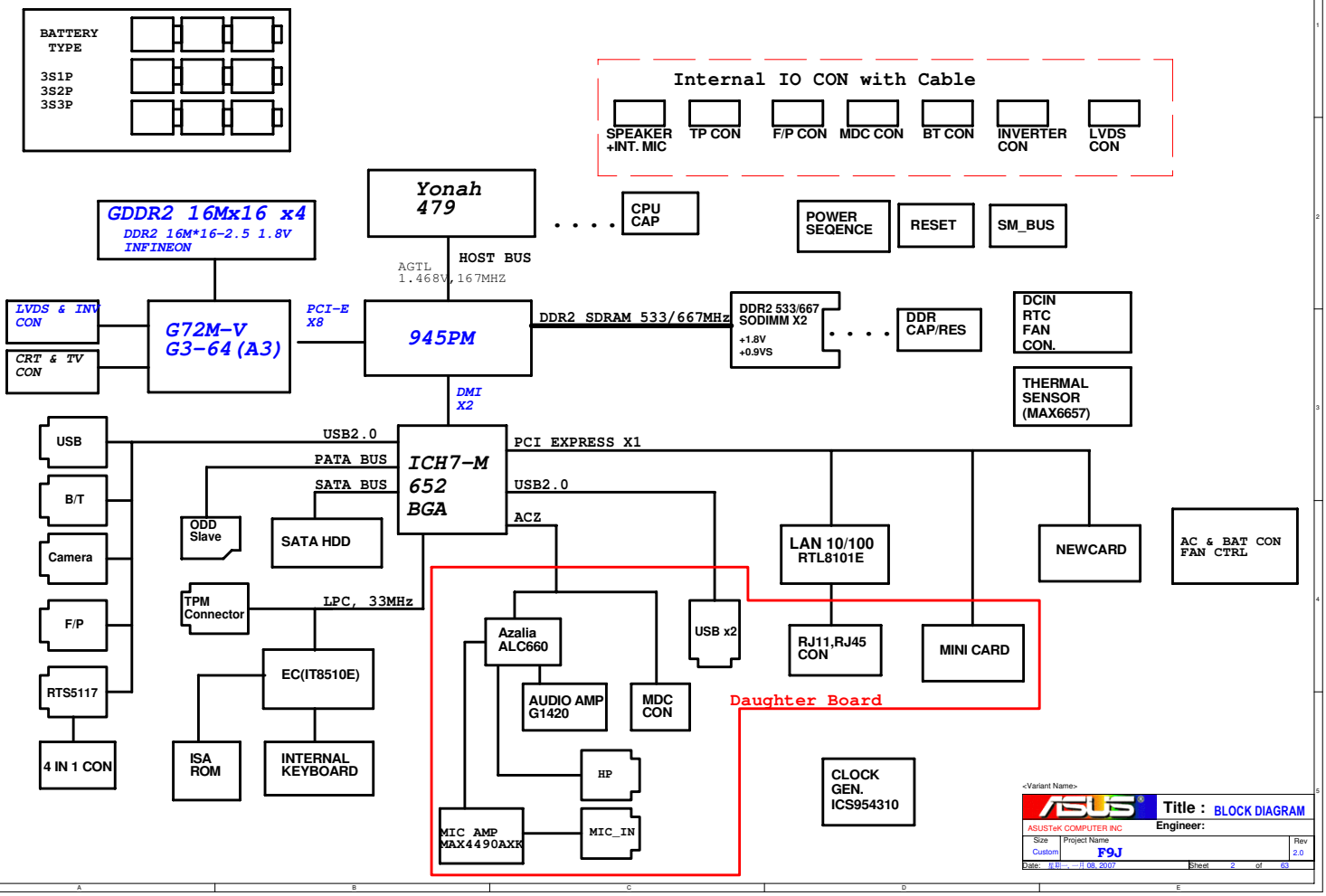
F9J BLOCK DIAGRAM



<< Kennedy_Zhang >>

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	N/A	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	N/A	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	N/A	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	BT_SW#	I
89	ADC6/GPE2	N/A	
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	BAT_AD	I
82	ADC1	ADP_ERR#	I
83	ADC2	AC_AD	I
84	ADC3	N/A	
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)--CPU	1001100x (98)
Thermal Sensor(G781-1)--VGA	1001101x (9A)

PCI Device	IDSEL#	REQ/GNT#	Interrupts

ICH7M_GPIO

Pin		Use As	Signal Name	Power
GPIO 00	i	GPI	PM_BMBUSY#	+3VS
GPIO 01	i	GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i	GPO	BT_LED_EN	+3VS
GPIO 07	i	GPI	RF_ON_SW#	+3VS
GPIO 08	i	GPI	EXTSMI#	+3VSUS
GPIO 09	i	GPI	N/A	+3VSUS
GPIO 10	i	GPI	N/A	+3VSUS
GPIO 11	i	Native	SMB_ALERT#	+3VSUS
GPIO 12	i	GPI	KBC_SCI#	+3VSUS
GPIO 13	i	GPI	N/A	+3VSUS
GPIO 14	i	GPI	N/A	+3VSUS
GPIO 15	i	GPO	802_LED_EN	+3VSUS
GPIO 16	O	0 GPO	PM_DPRSLPVR	+3VS
GPIO 17	O	1 GPO	PCI_GNT#5	+3VS
GPIO 18	O	1 GPO	STP_PCI#	+3VS
GPIO 19	i	1 GPI	N/A	+3VS
GPIO 20	O	1 GPO	STP_CPU#	+3VS
GPIO 21	i	1 GPO	N/A	+3VS
GPIO 22	i	1 Native	PCI_REQ#4	+3VS
GPIO 23	i	1 Native	N/A	+3VS
GPIO 24	O	0 GPO	MSK_PCIRST	+3VSUS
GPIO 25	O	1 GPO	N/A	+3VSUS
GPIO 26	O	0 GPO	BT_ON#	+3VSUS
GPIO 27	O	0 GPO	WLAN_ON#	+3VSUS
GPIO 28	O	0 GPO	N/A	+3VSUS
GPIO 29	i	0 Native	USB_OC#5	+3VSUS
GPIO 30	i	0 Native	USB_OC#6	+3VSUS
GPIO 31	i	0 Native	USB_OC#7	+3VSUS
GPIO 32	O	1 GPO	PM_CLKRUN#	+3VS
GPIO 33	O	1 GPO	N/A	+3VS
GPIO 34	O	0 GPO	N/A	+3VS
GPIO 35	O	0 GPO	N/A	+3VS
GPIO 36	i	0 GPO	N/A	+3VS
GPIO 37	i	0 GPI	PCB_ID0	+3VS
GPIO 38	i	0 GPI	PCB_ID1	+3VS
GPIO 39	i	0 GPI	PCB_ID2	+3VS
GPIO [40:47]		NA	NA	NA
GPIO 48		Native	PCI_GNT#4	+3VS
GPIO 49		Native	H_PWRGD	+VCORE

<Variant Name>

ASUSTeK COMPUTER INC

Title : Schematic data

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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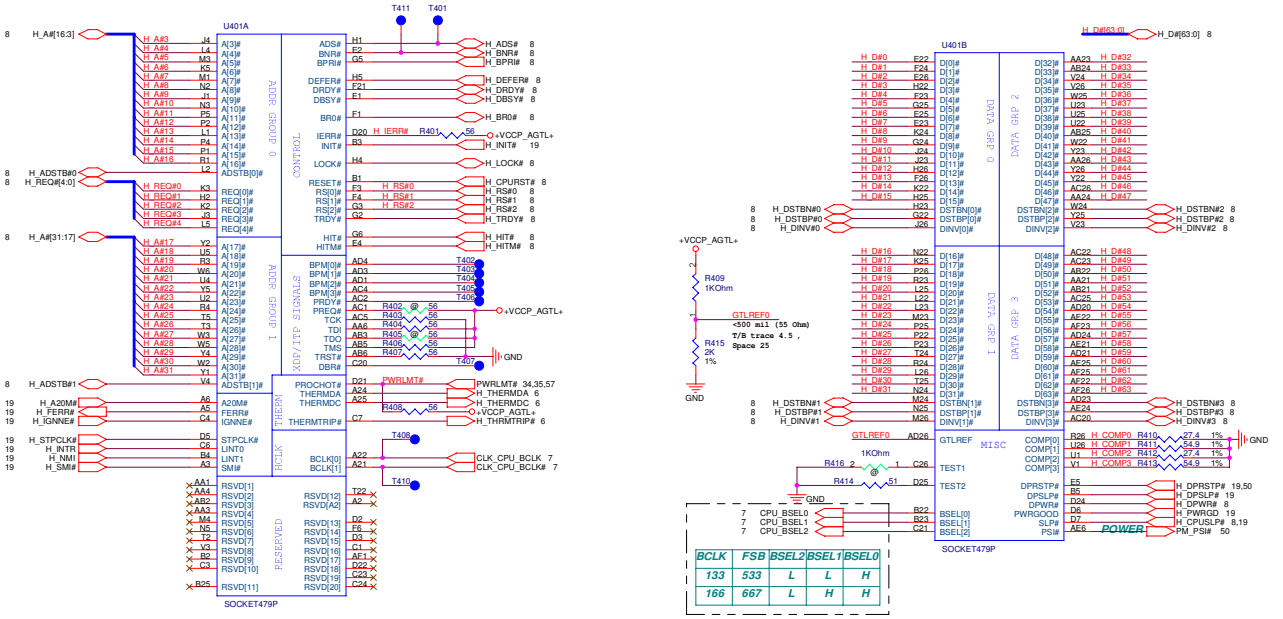

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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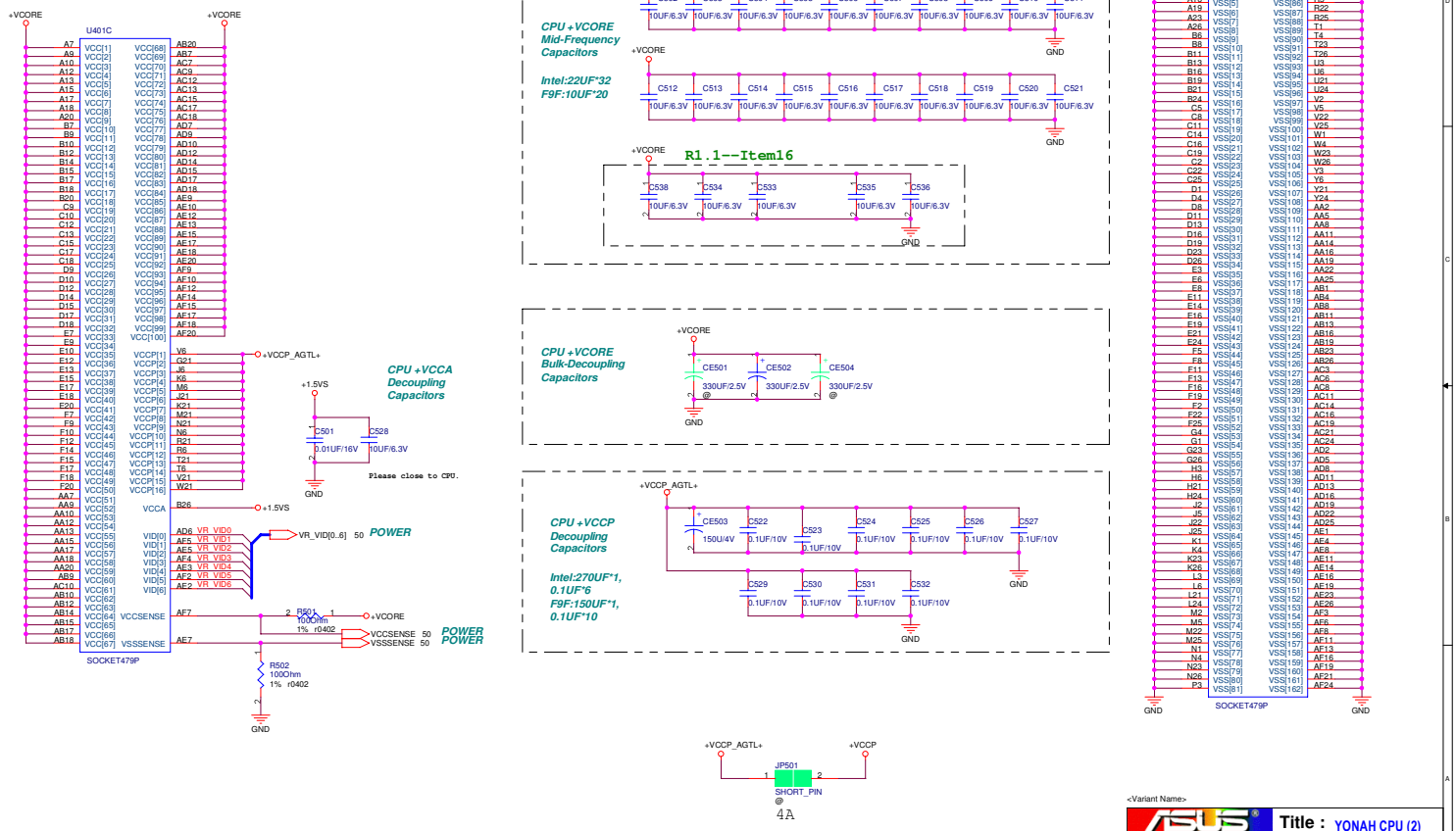

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (2)

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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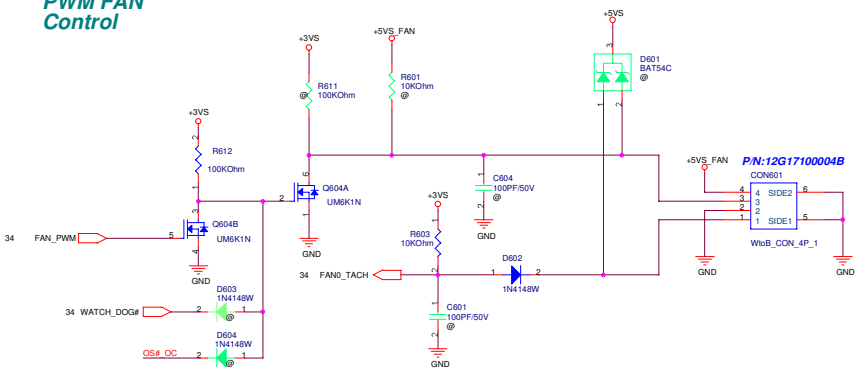
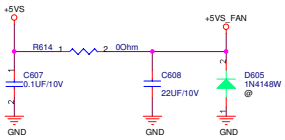
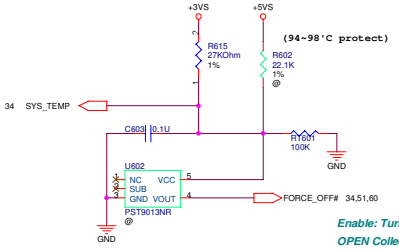
PWM FAN Control



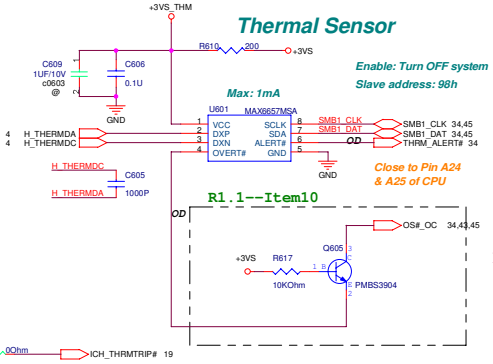


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC



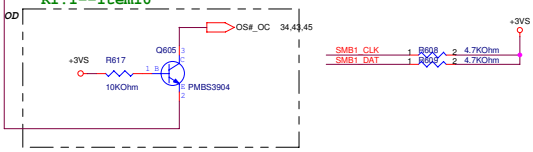
Enable: Turn OFF system
OPEN Collect

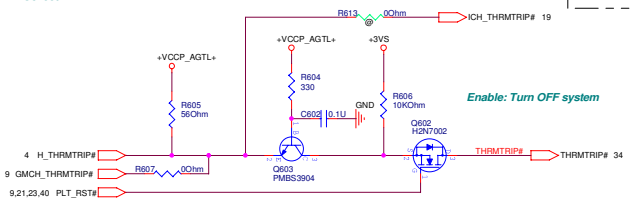
Thermal Sensor



Enable: Turn OFF system
Slave address: 98h
Max: 1mA
Close to Pin A24 & A25 of CPU

R1.1--Item10





Enable: Turn OFF system

<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN_CTRL&Thernal	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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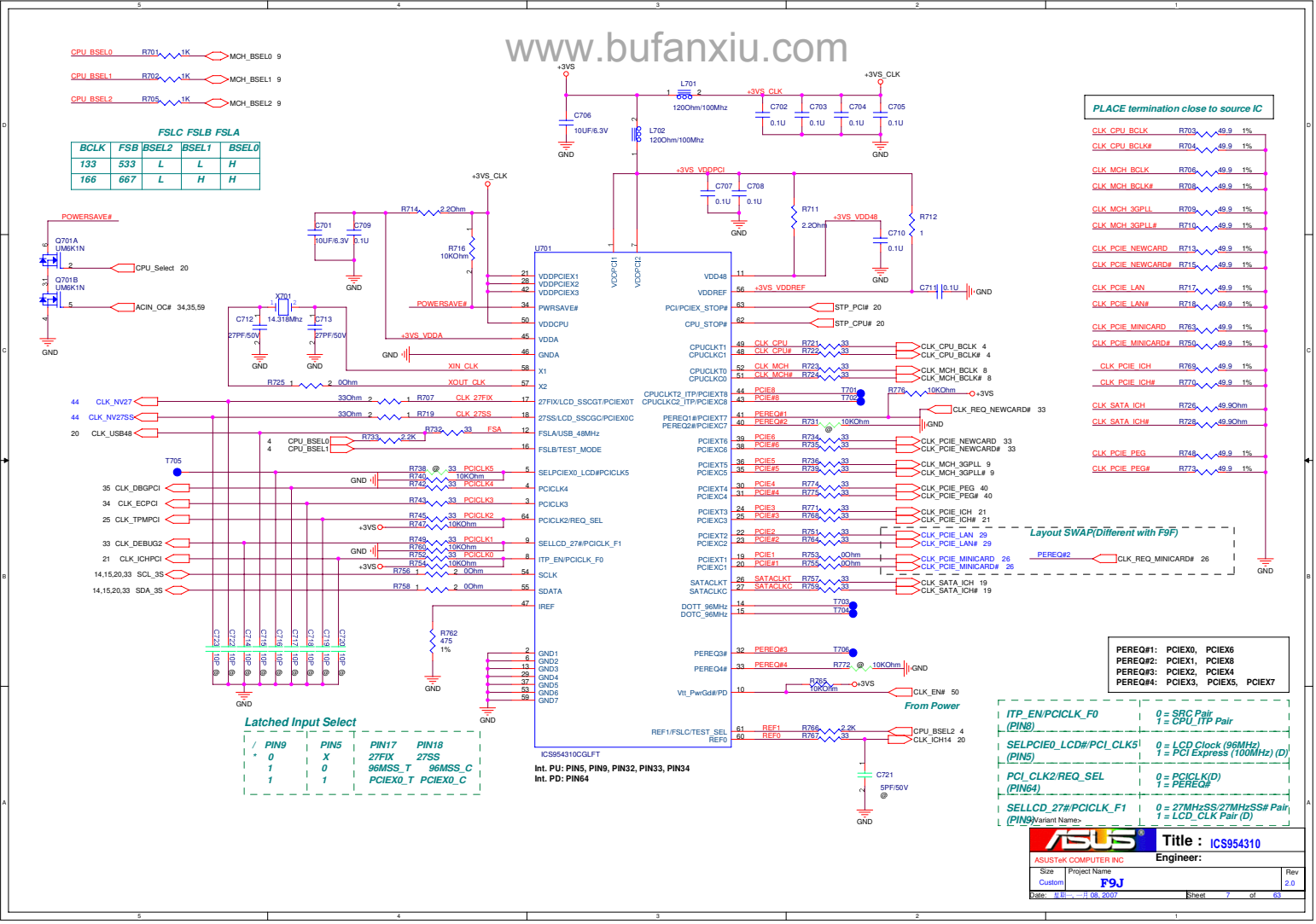

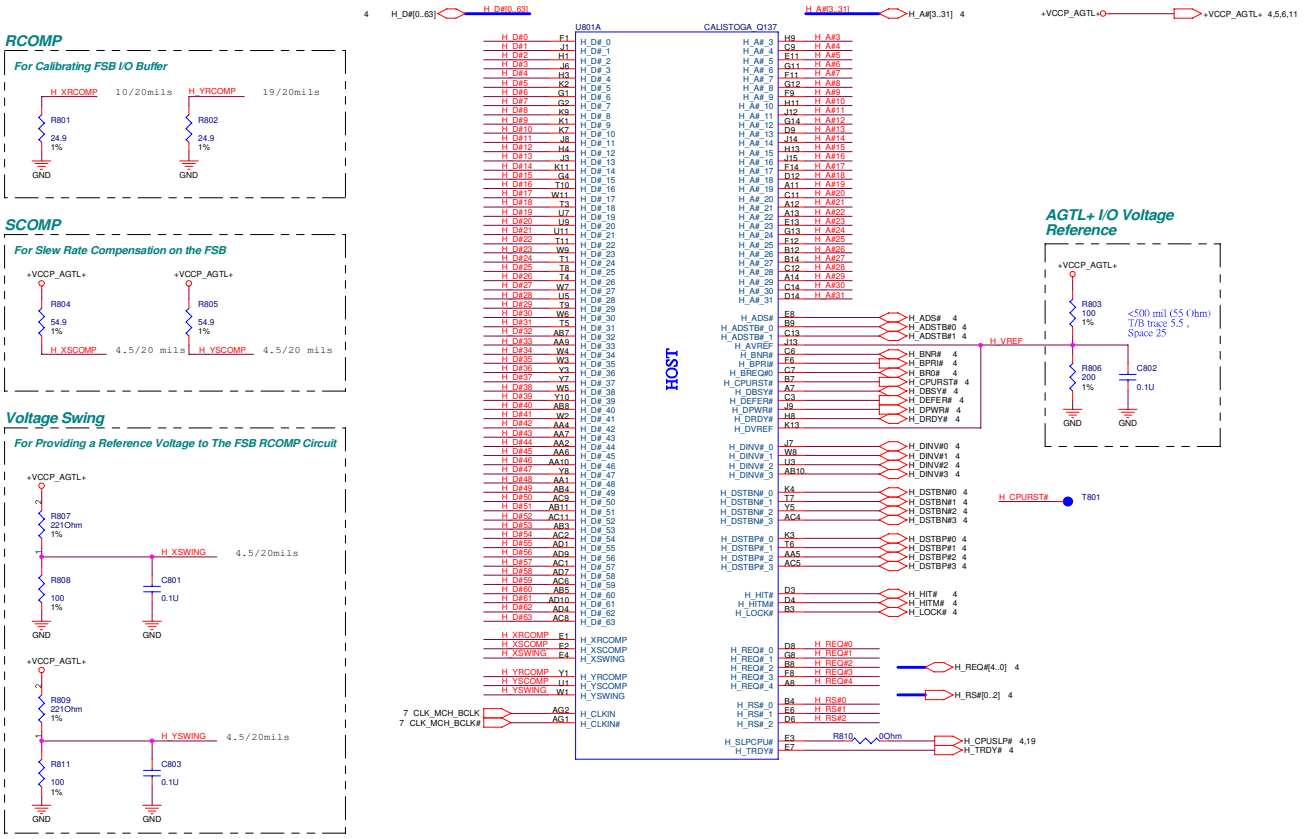

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--CPU

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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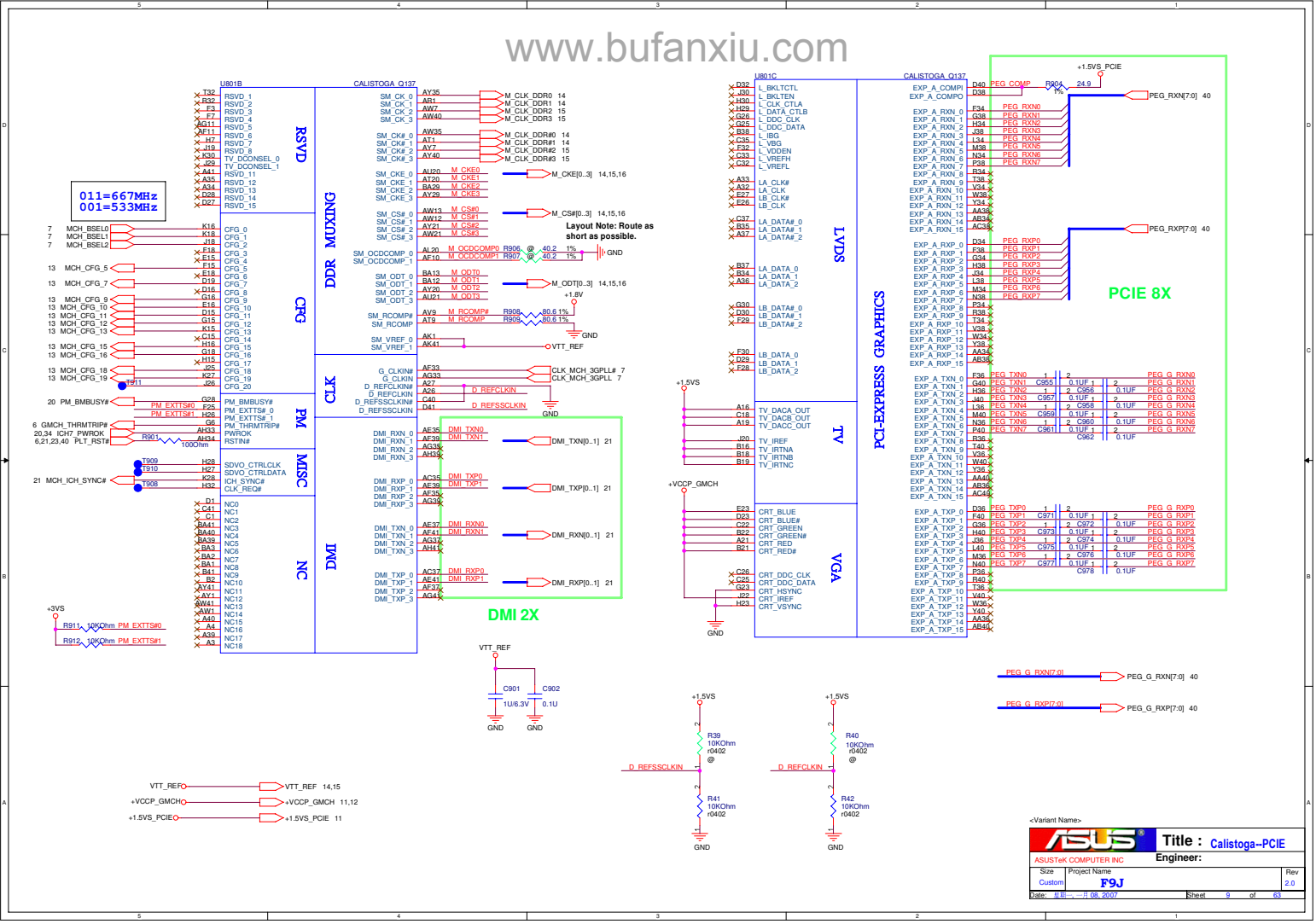

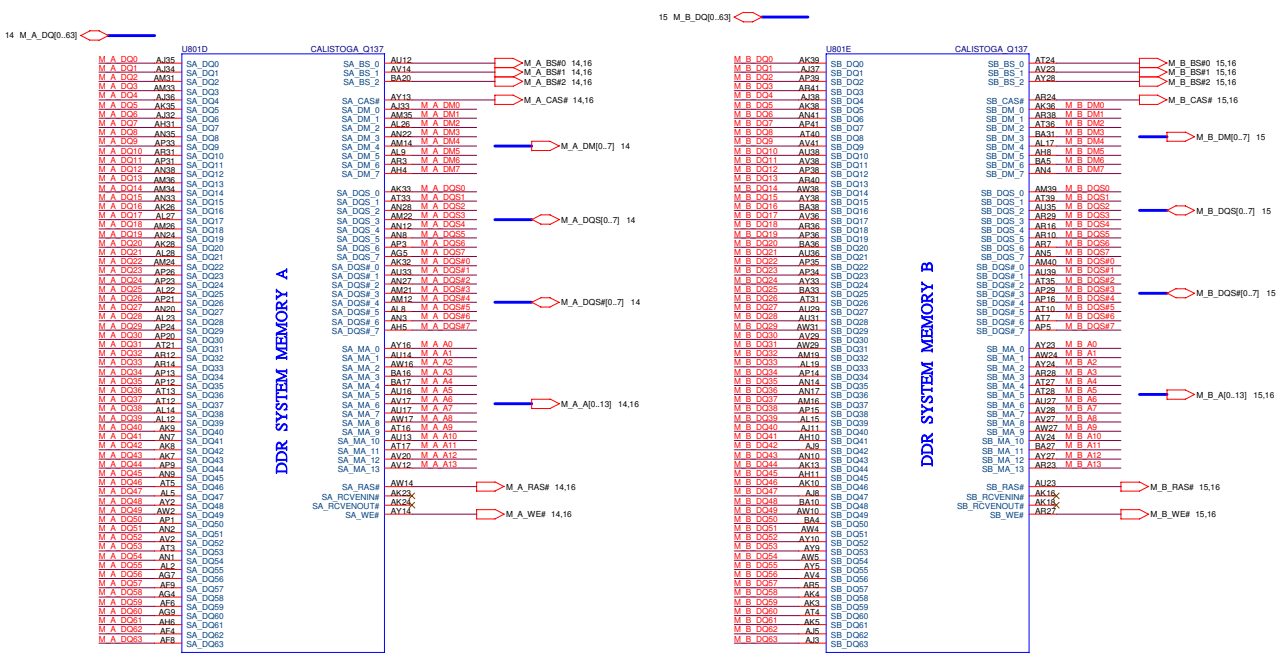

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--DDR2

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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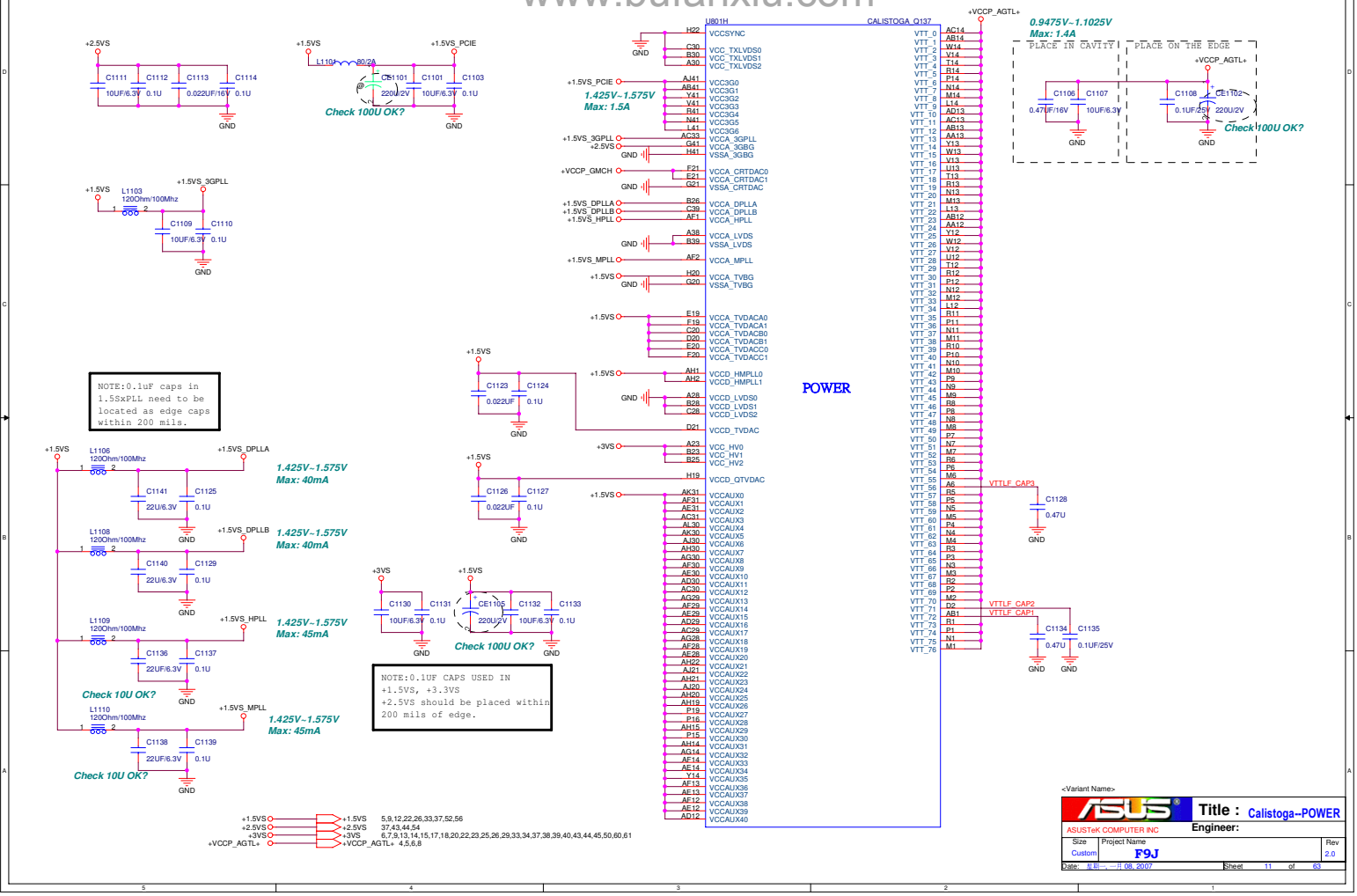

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--POWER

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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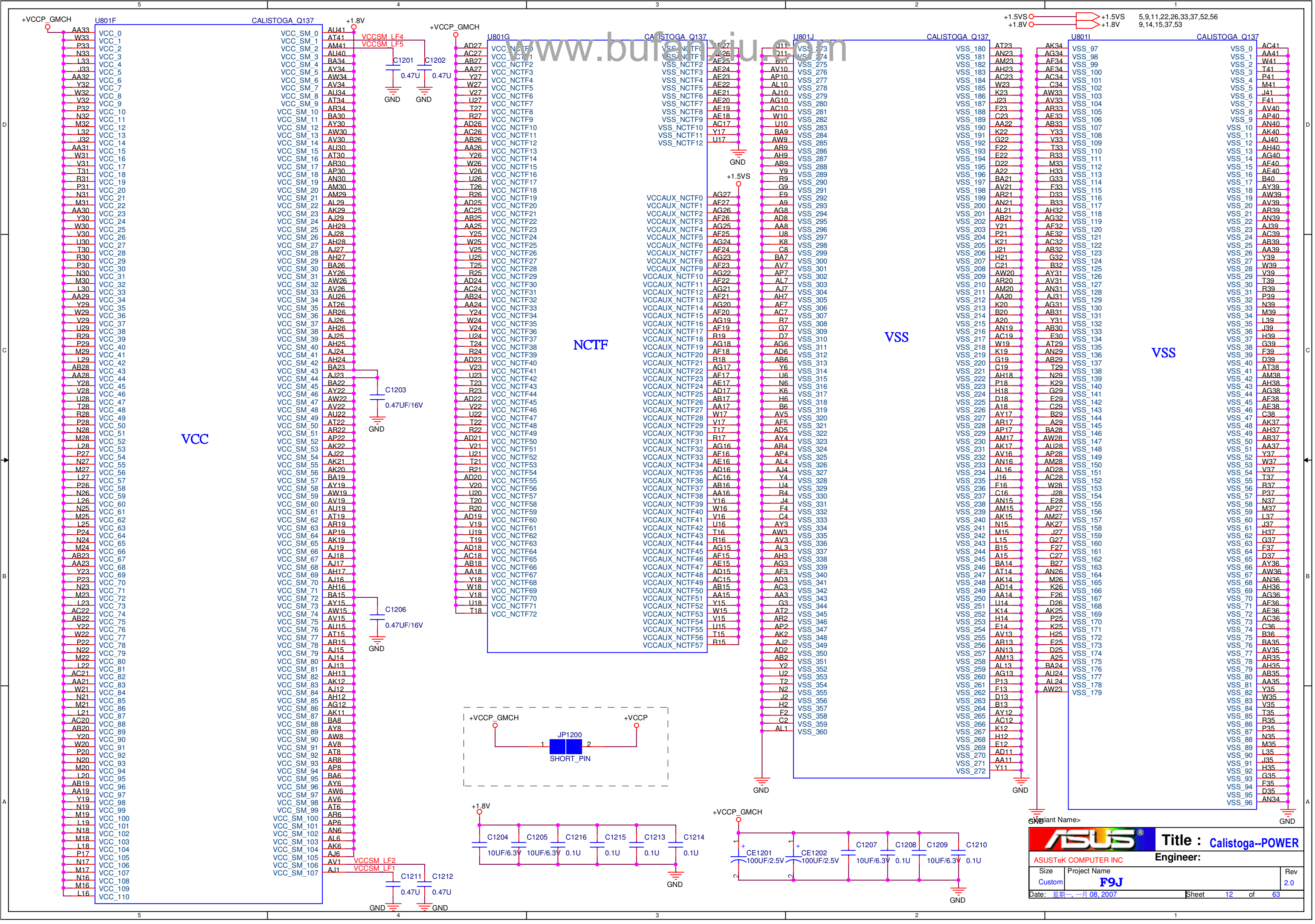
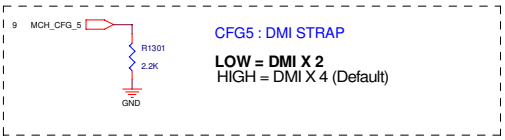
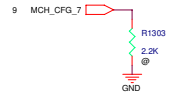


+3VS >> 3VS 6,7,9,11,14,15,17,18,20,22,23,25,26,29,33,34,37,38,39,40,43,44,45,50,60,61



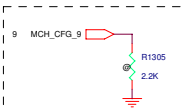
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



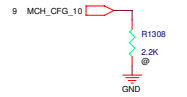
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



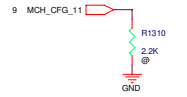
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

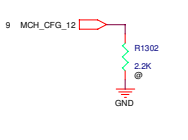
LOW = RESERVED
HIGH = MOBILITY (Default)



CFG11 : PSB 4x CLK ENABLE

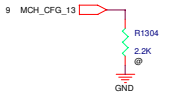
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

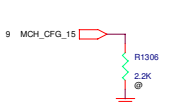
```
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.
```



CFG[13:12] : GMCH TEST MODE SELECT

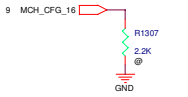
00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)





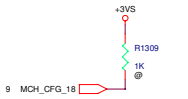
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



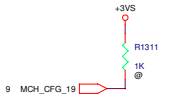
CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
HIGH = LANES REVERSED

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--Strap

Engineer:

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Custom	F9J	2.0

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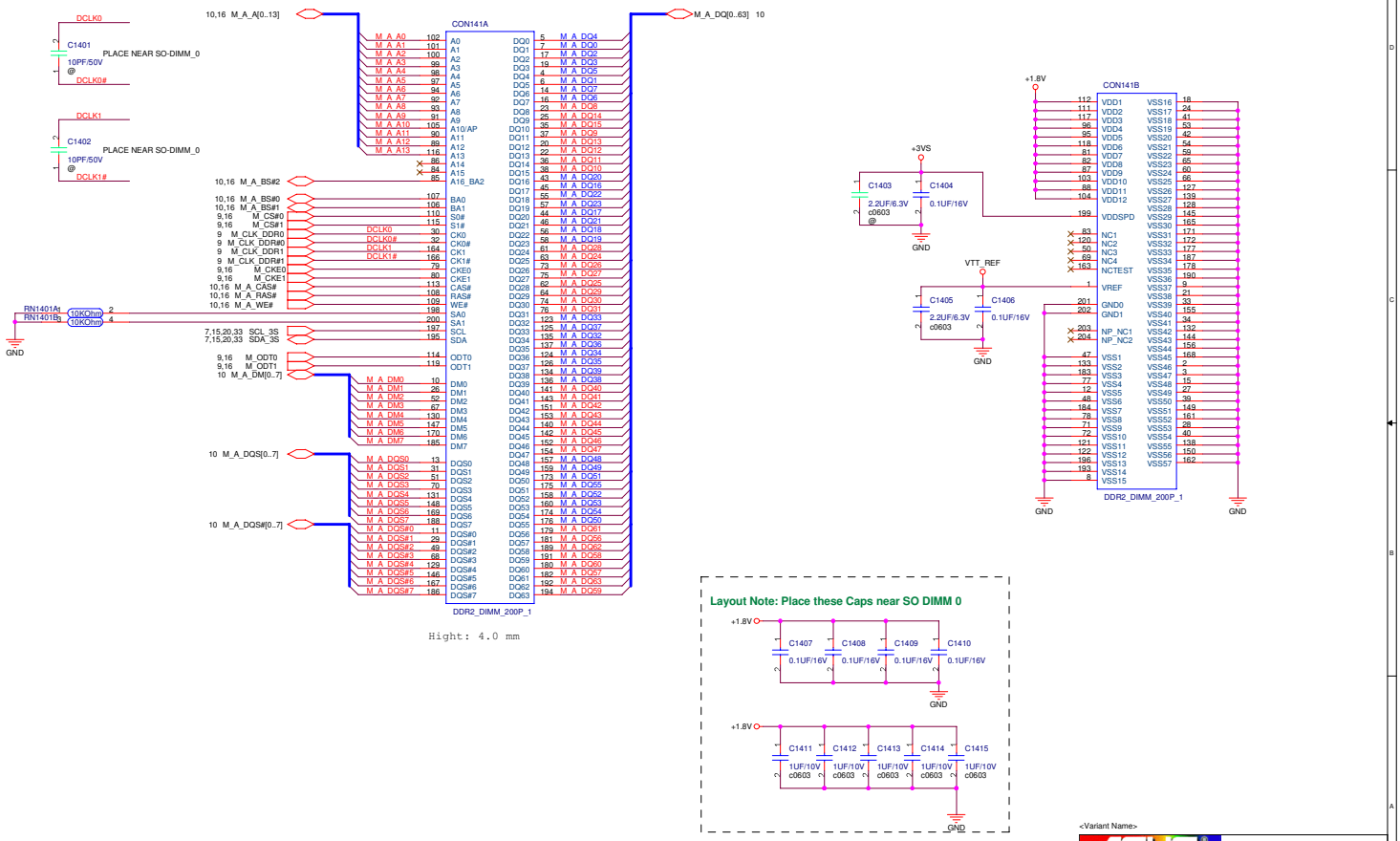

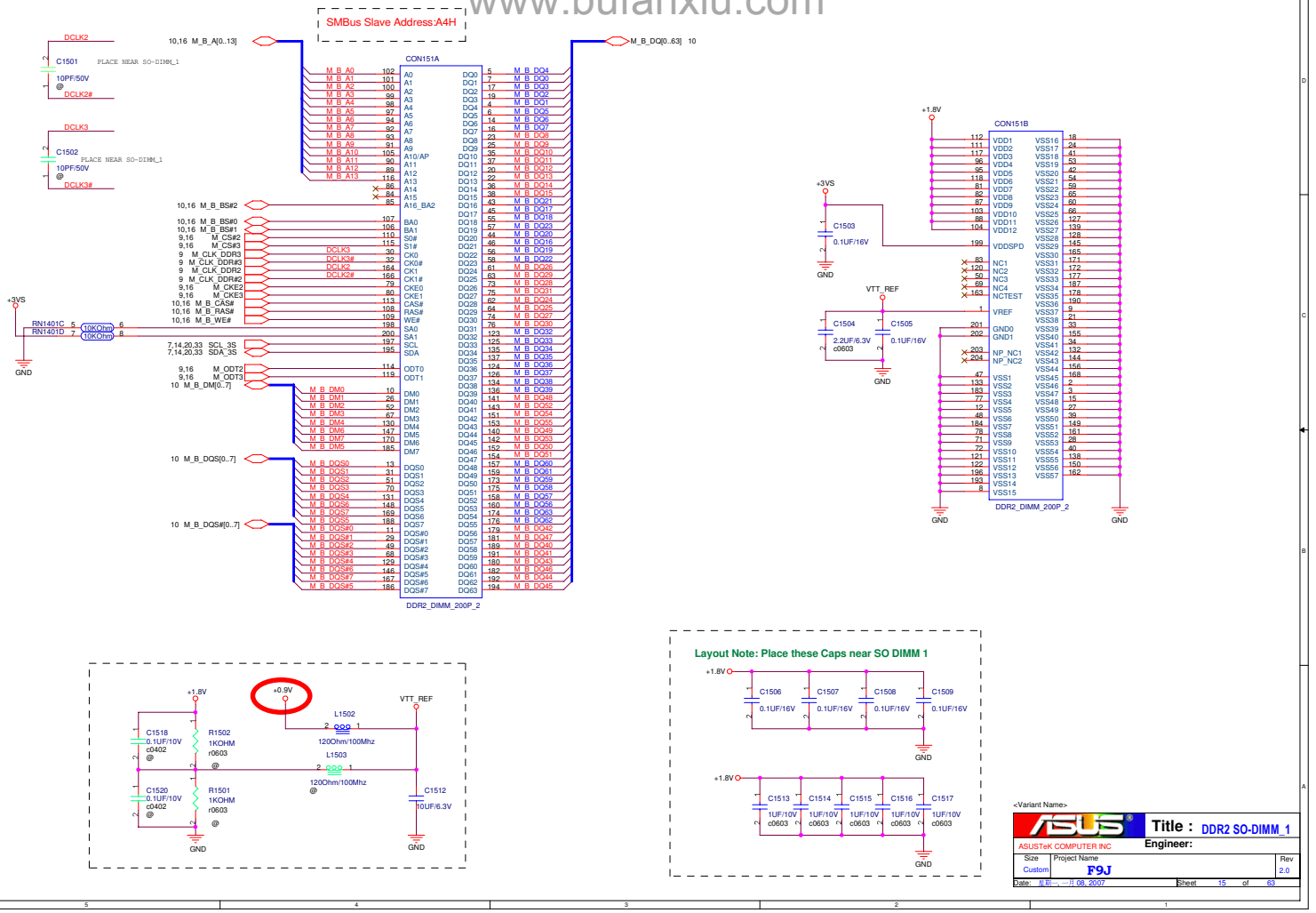

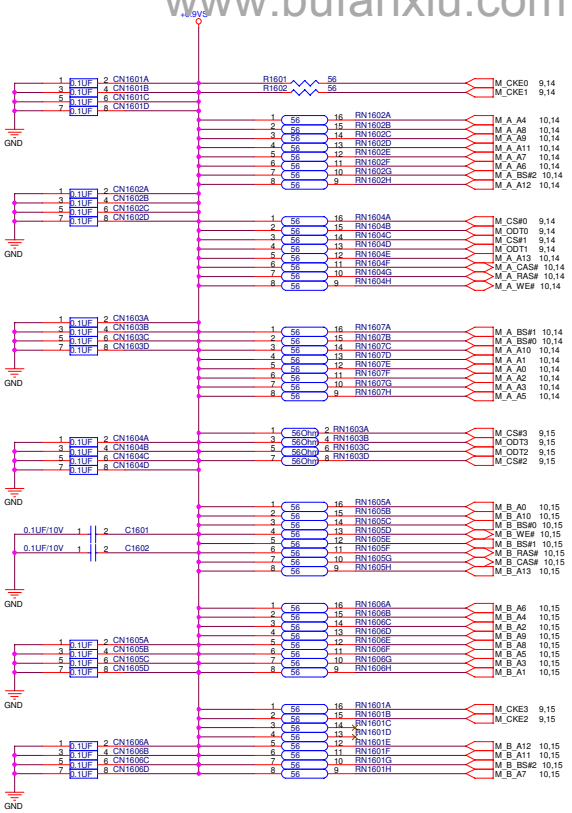

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

Title :DDR2 TERMINATION

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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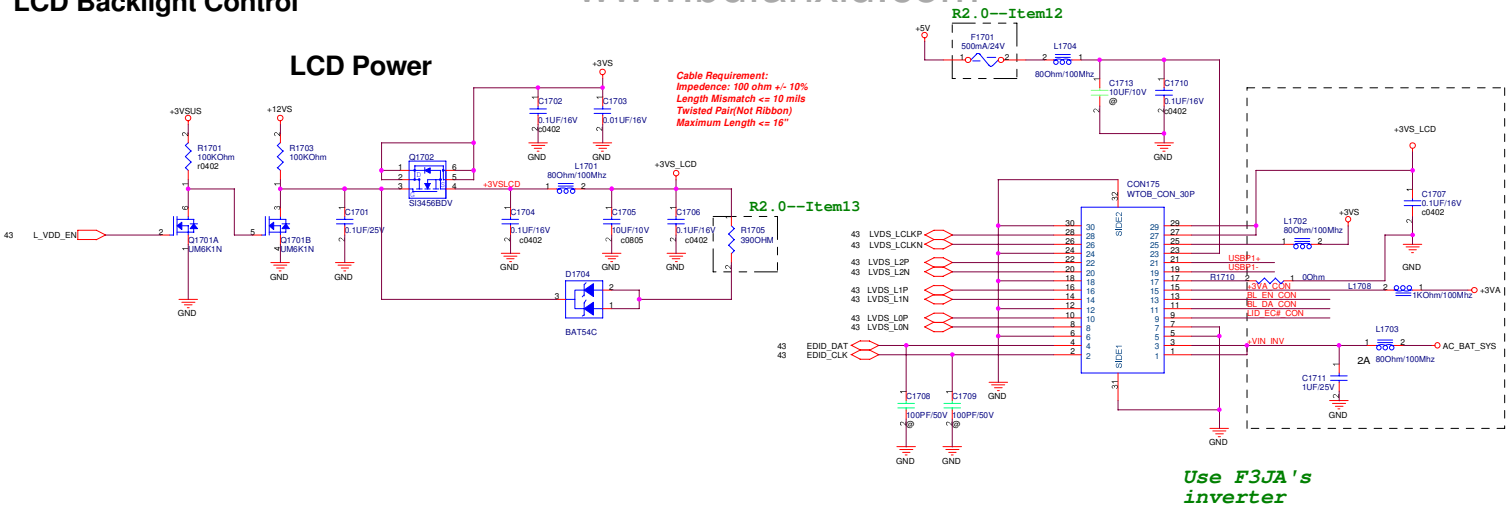
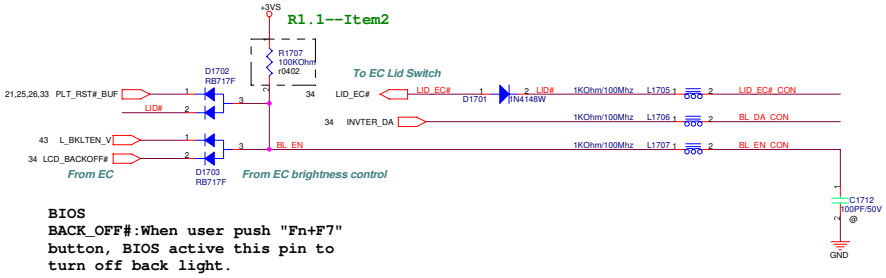
LCD Backlight Control

LCD Power

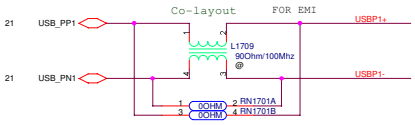


Use F3JA's inverter

CCD connecter

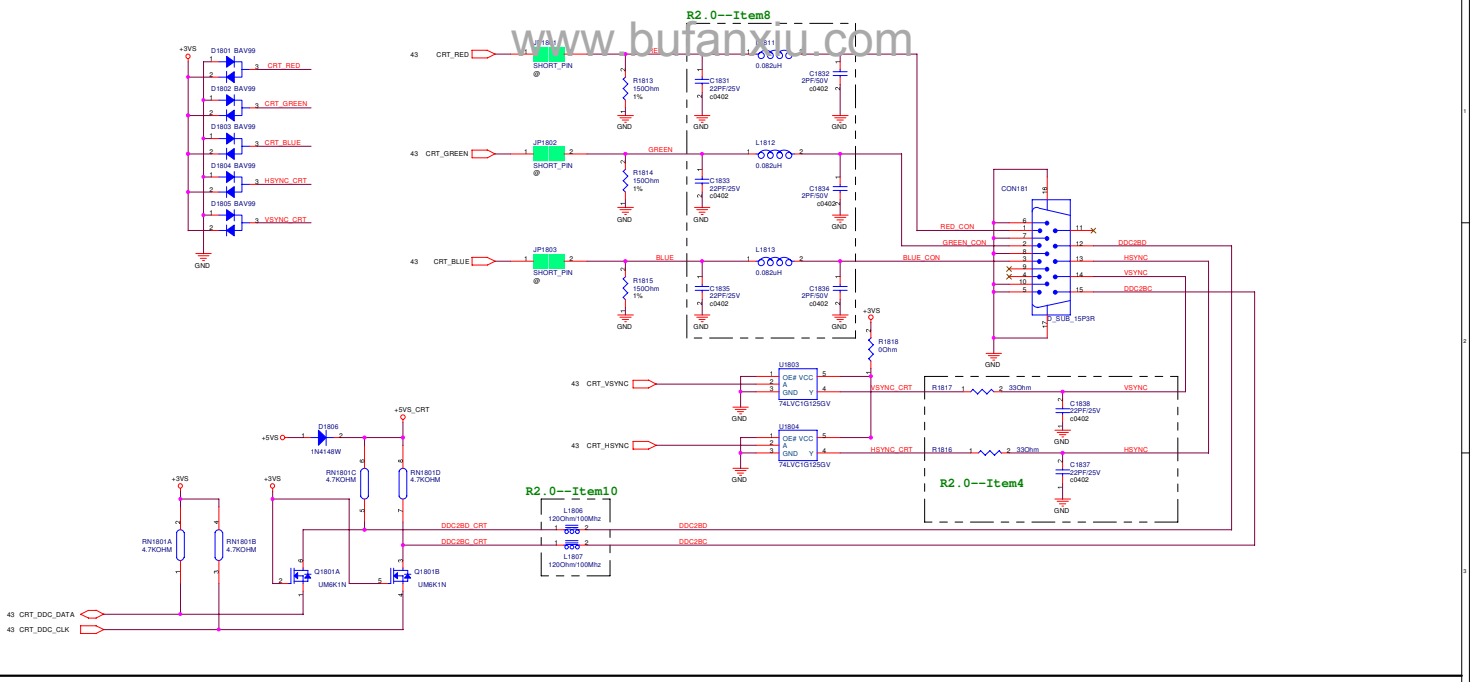


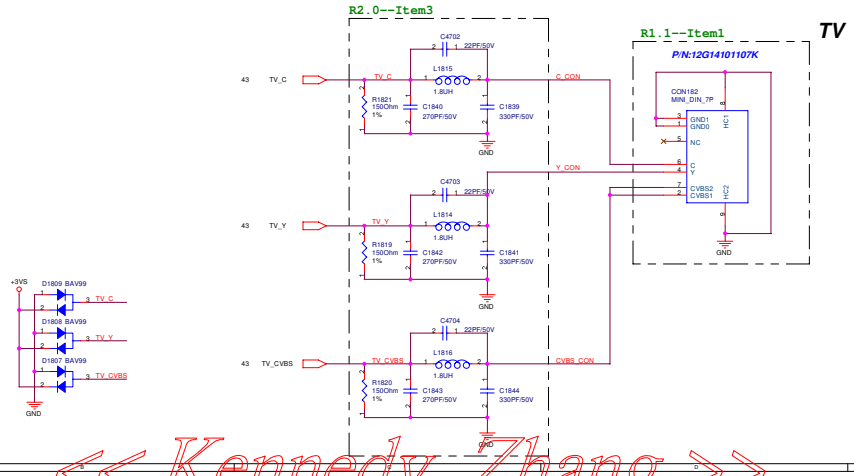
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: 非日一, 一月 08, 2007	Sheet 17 of 63	





<Variant Name>

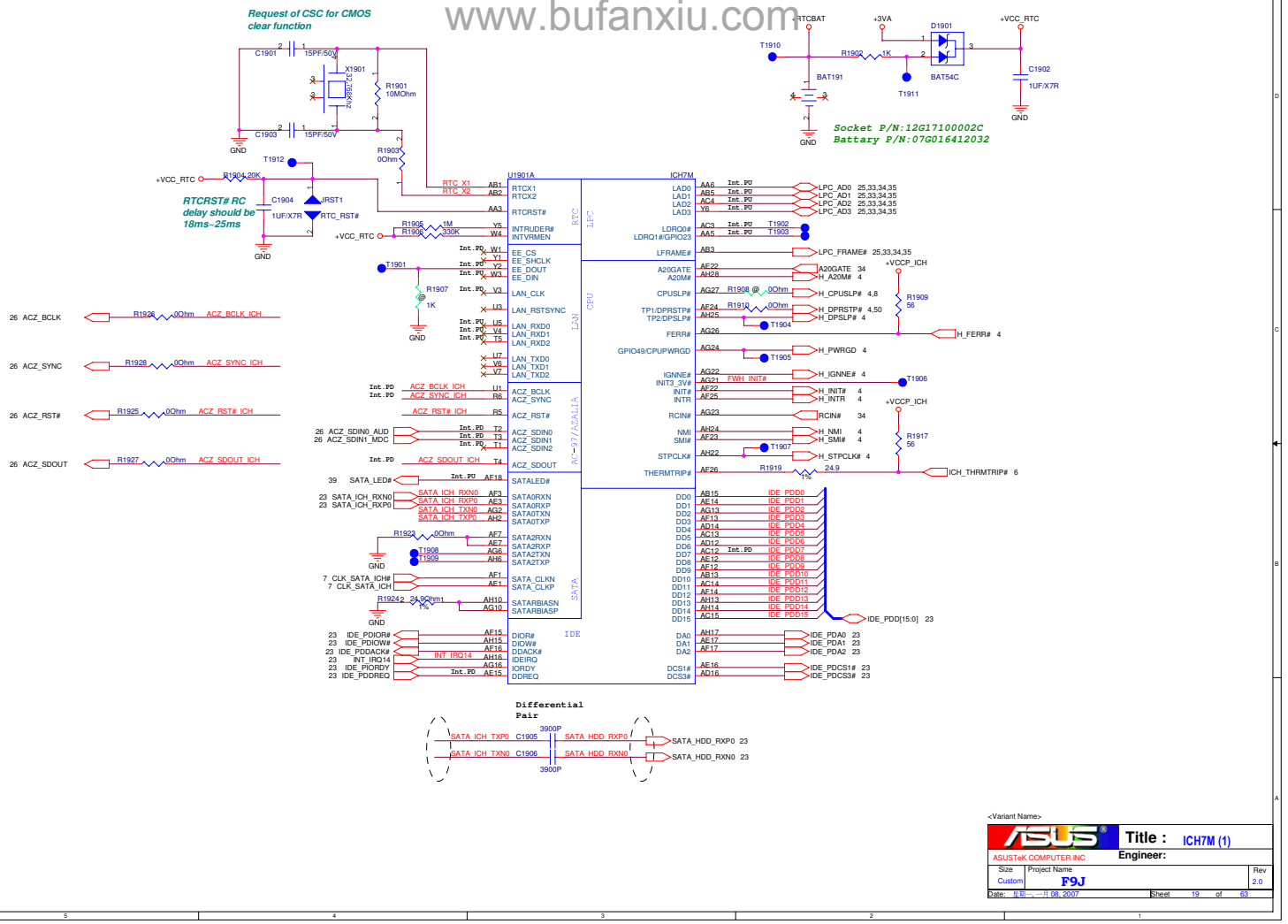
ASUSTeK COMPUTER INC

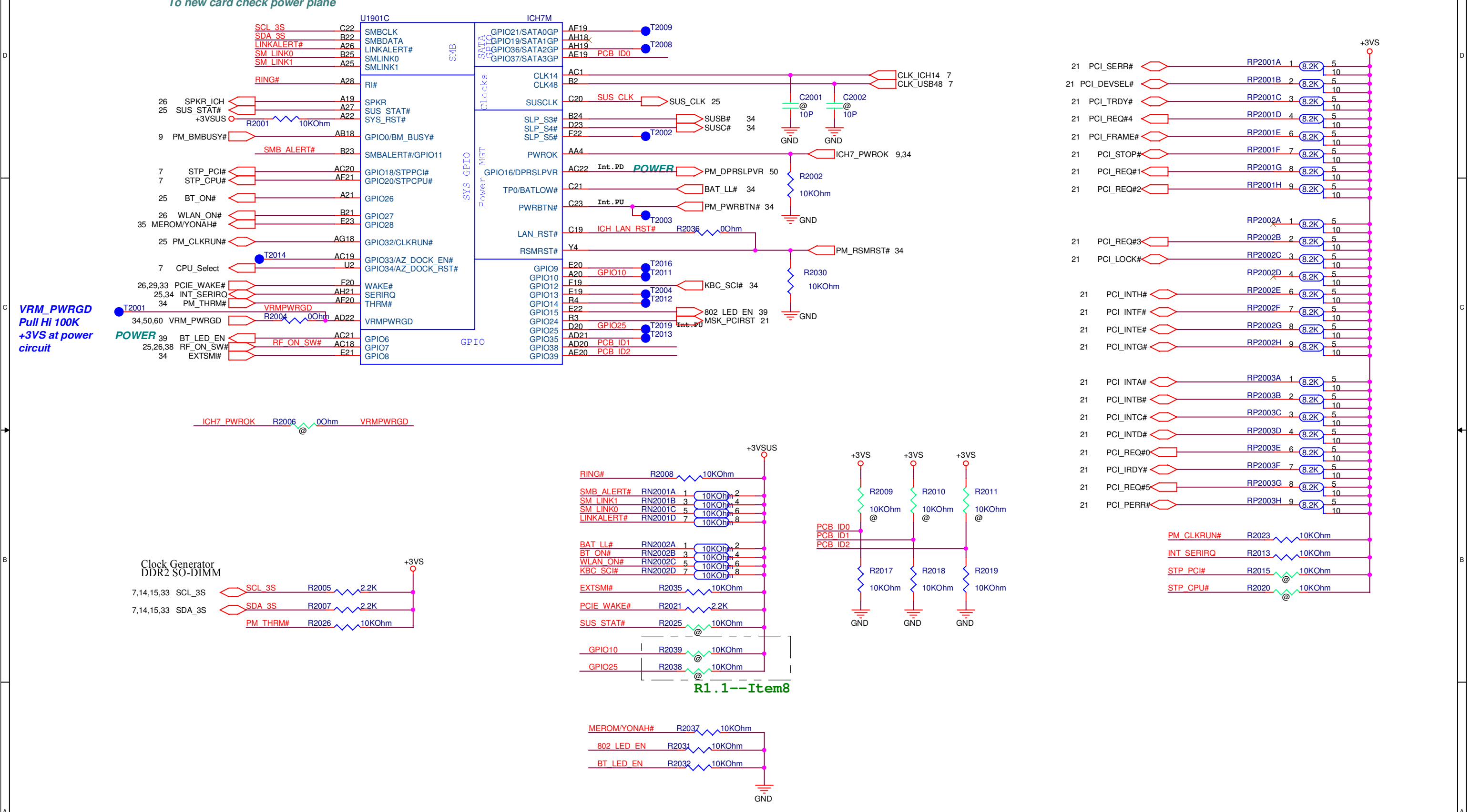
Title : CRT & TV OUT

Engineer:

Size	Project Name	Rev
C	F9J	2.0

Date: 星期一, 08, 2007 Sheet 18 of 63





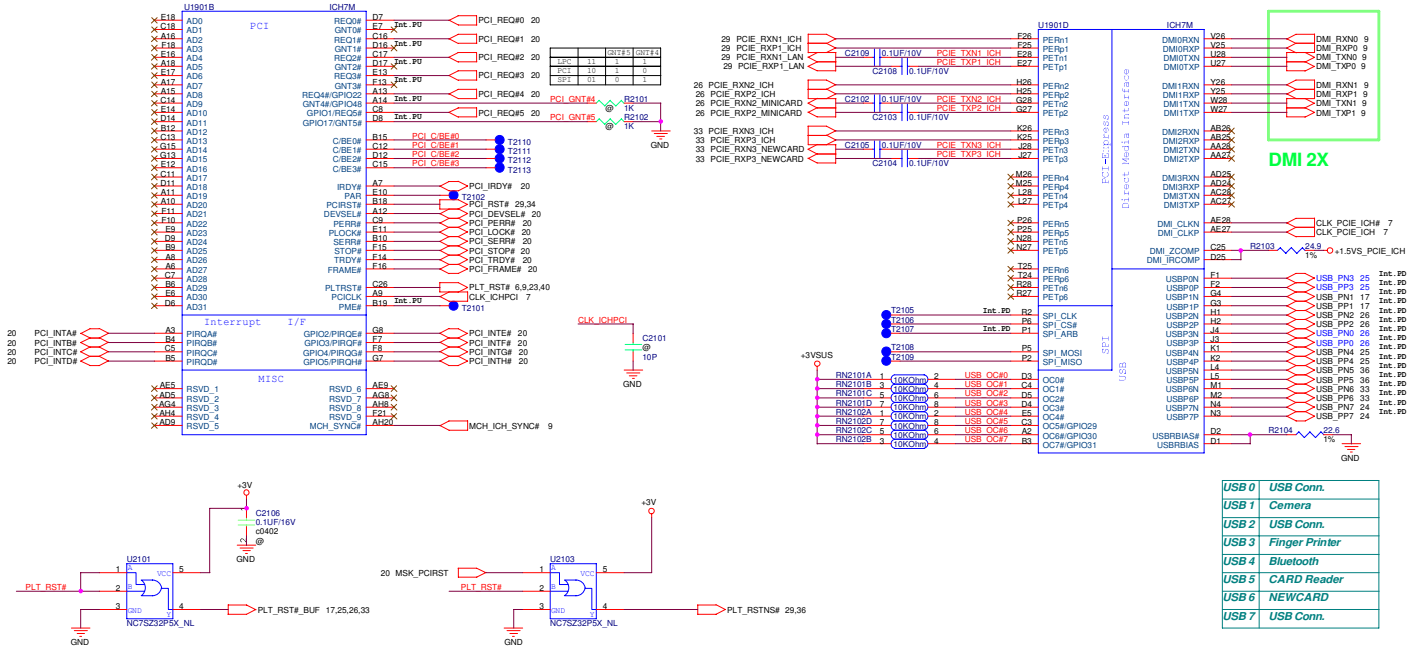
Title : ICH7M (2)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: 星期一, 一月 08, 2007 Sheet 20 of 63



USB 0	USB Conn.
USB 1	Cemera
USB 2	USB Conn.
USB 3	Finger Printer
USB 4	Bluetooth
USB 5	CARD Reader
USB 6	NEWCARD
USB 7	USB Conn.

<Variant Name>

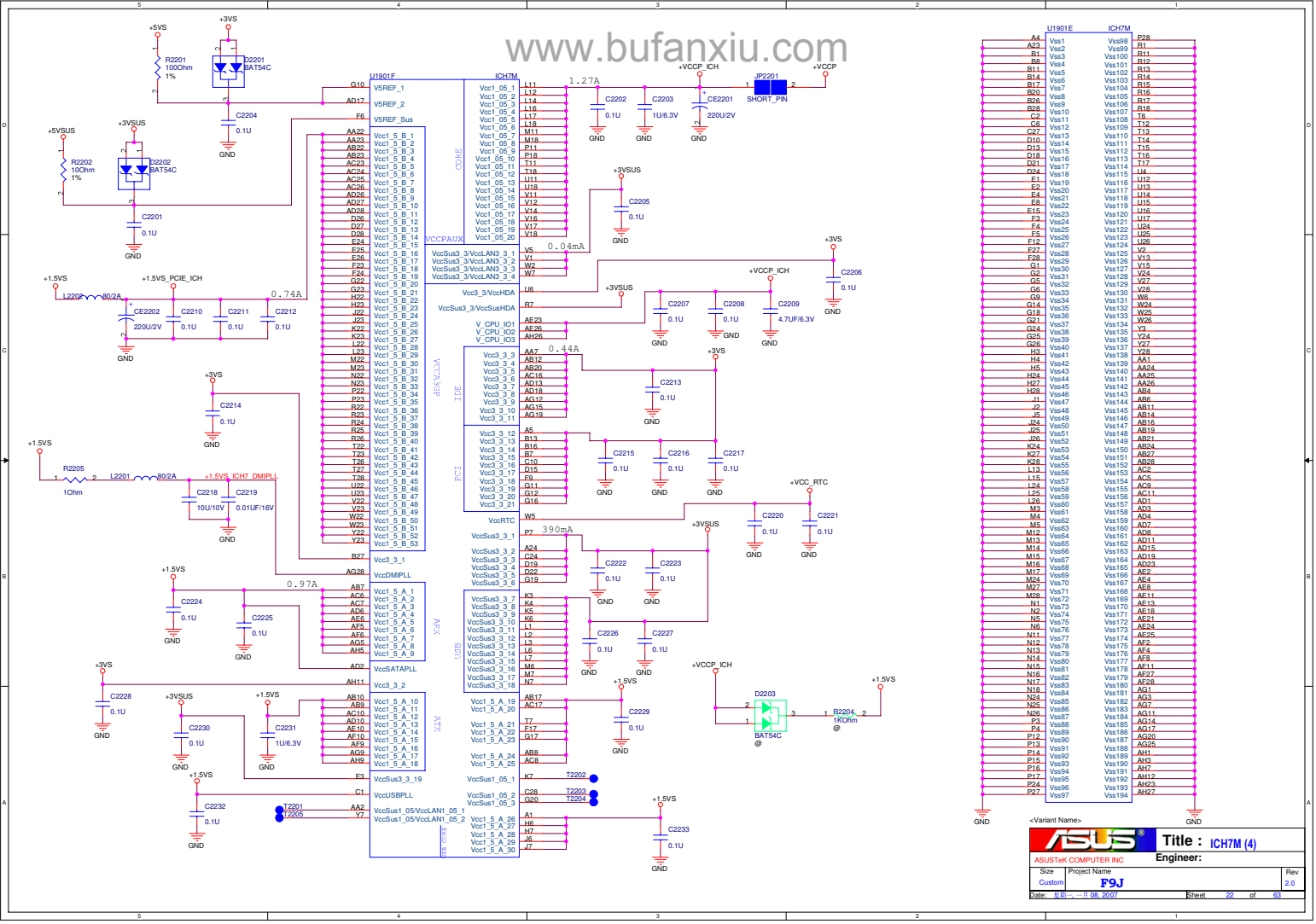
ASUSTeK COMPUTER INC

Title : ICH7M (3)

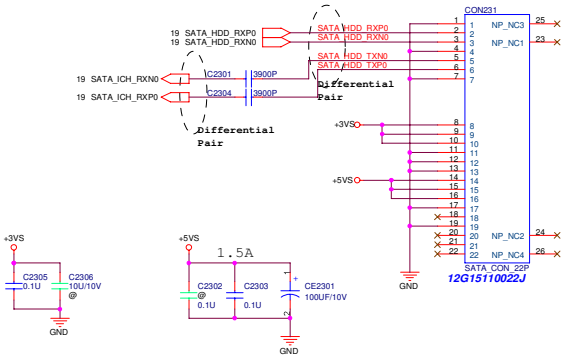
Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: 星期一, 一月 08, 2007 Sheet 21 of 63

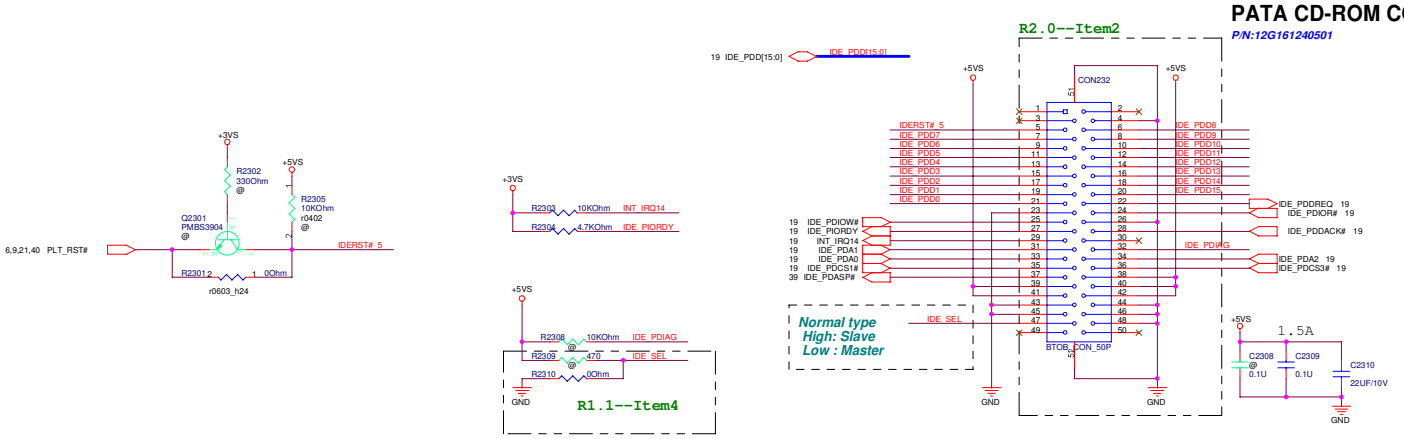


SATA HDD CON



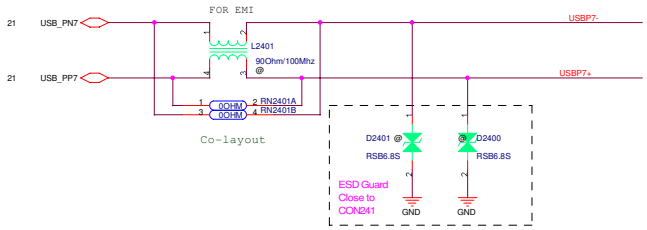
PATA CD-ROM CON

P/N:12G161240501

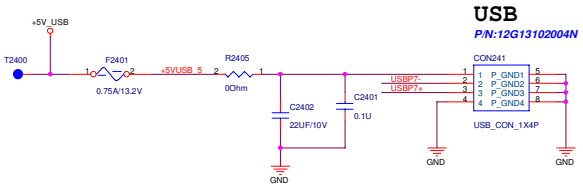


<Variant Name>

Title :	HDD & CDROM
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name: F9J
Rev: 2.0	
Date: 日 08, 2007	Sheet 23 of 63

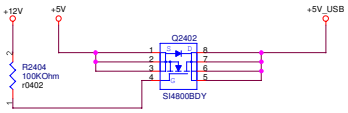


Change ESD package for layout placement.



USB

P/N:12G13102004N



<Variant Name>

ASUSTeK COMPUTER INC

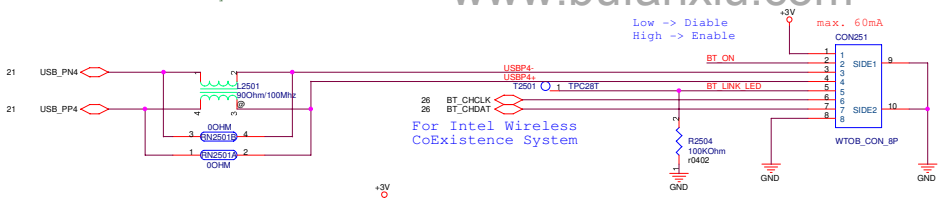
Title : USB PORTS

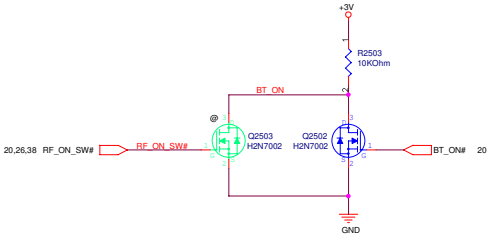
Engineer:

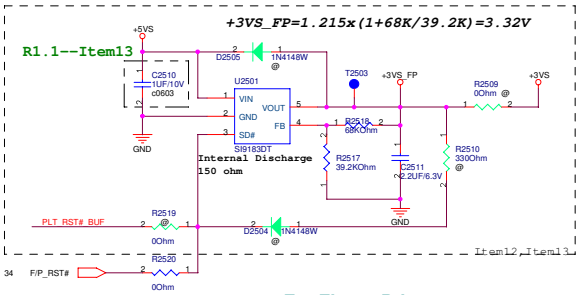
Size	Project Name	Rev
Custom	F9J	2.0

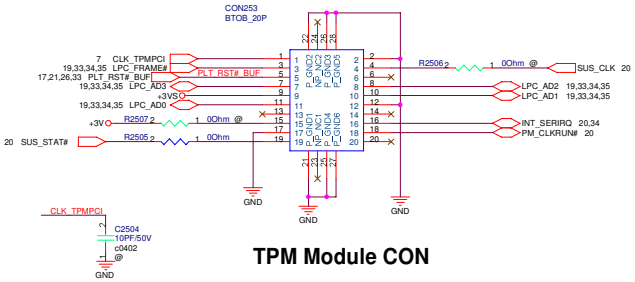
Date: 日 8, 2007 Sheet 24 of 63

Co-layout FOR EMI

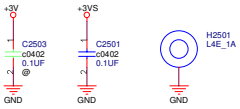




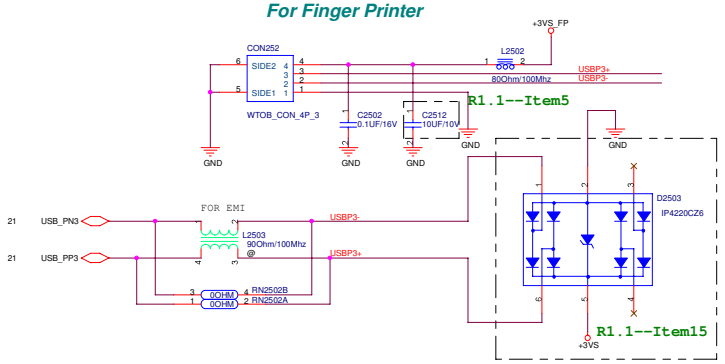




TPM Module CON



For Finger Printer



<Variant Name>

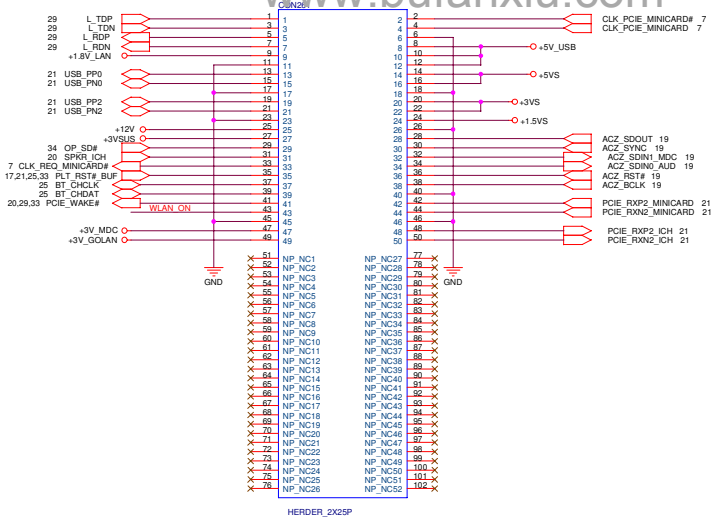
ASUSTeK COMPUTER INC	Title : B/T,F/P& TPM	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: 日 8, 2007	Sheet 25 of 63	

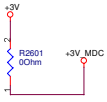
POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS:+1.425V~+1.575V
Max= 375 mA

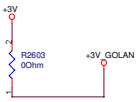
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC:+3.003V~+3.597V
Max= 300 mA



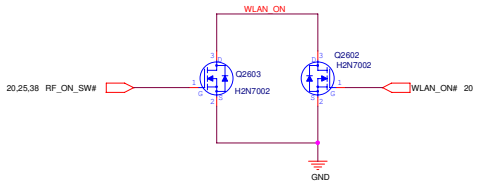


Reserved R to +3VSUS for Wake on RING function!



Reserved R to +3VSUS for Wake on WLAN function!

Intel SPEC(18780):Internal Pull UP 110Kohm



<Variant Name>

ASUSTeK COMPUTER INC

Title : B TO B CONN(M)

Engineer:

Size	Project Name	Rev
Custom		2.0

Date: 日 8, 2007 Sheet 26 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9F	2.0

Date: 日 08, 2007 Sheet 27 of 63

<Variant Name>

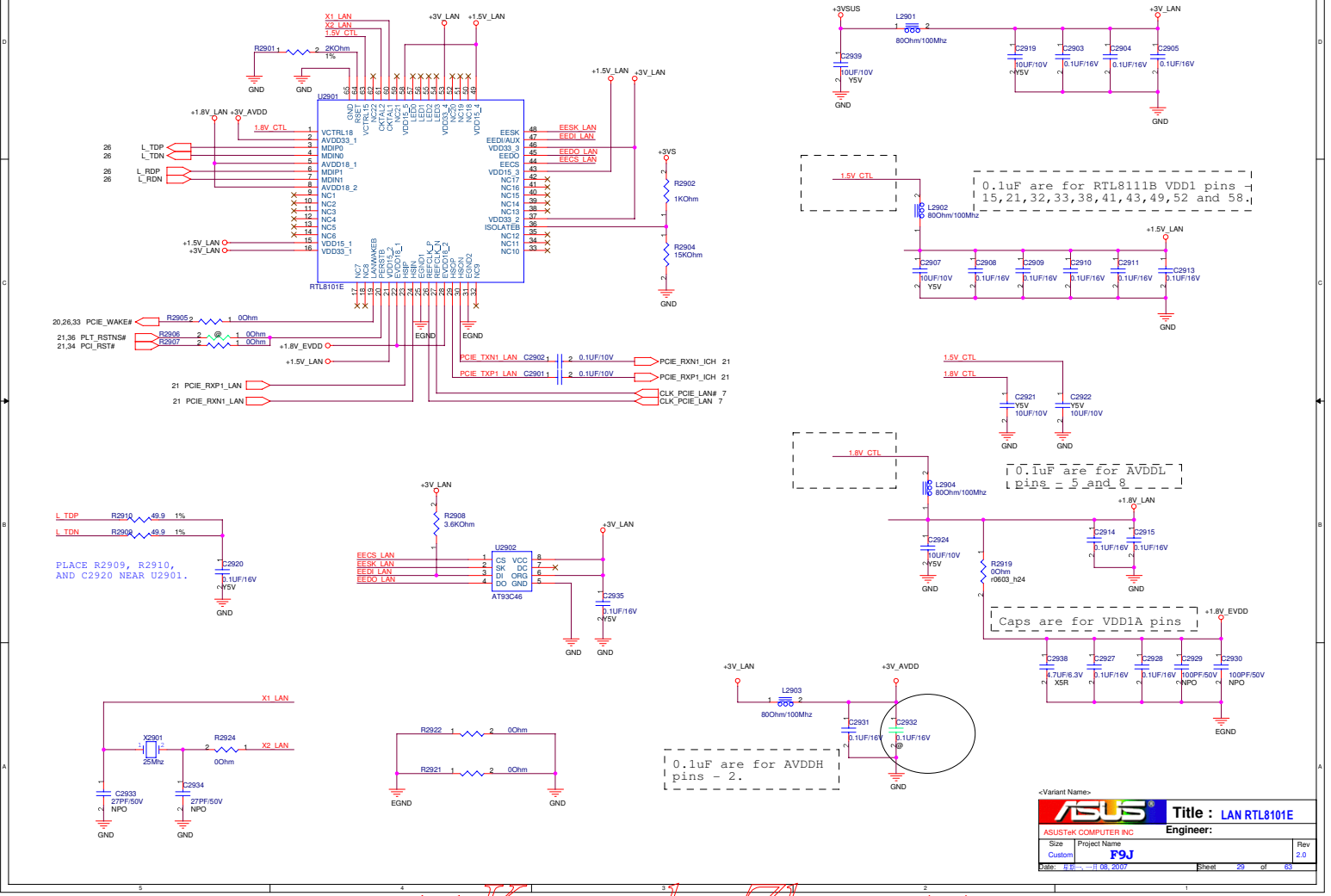
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9F	2.0

Date: 日 四一, 一月 08, 2007 Sheet 28 of 63



Title : EMPTY

ASUSTek COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: 星期一, 一月 08, 2007 Sheet 30 of 63

Title : EMPTY

ASUSTek COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: 星期一, 一月 08, 2007 Sheet 31 of 63

<Variant Name>

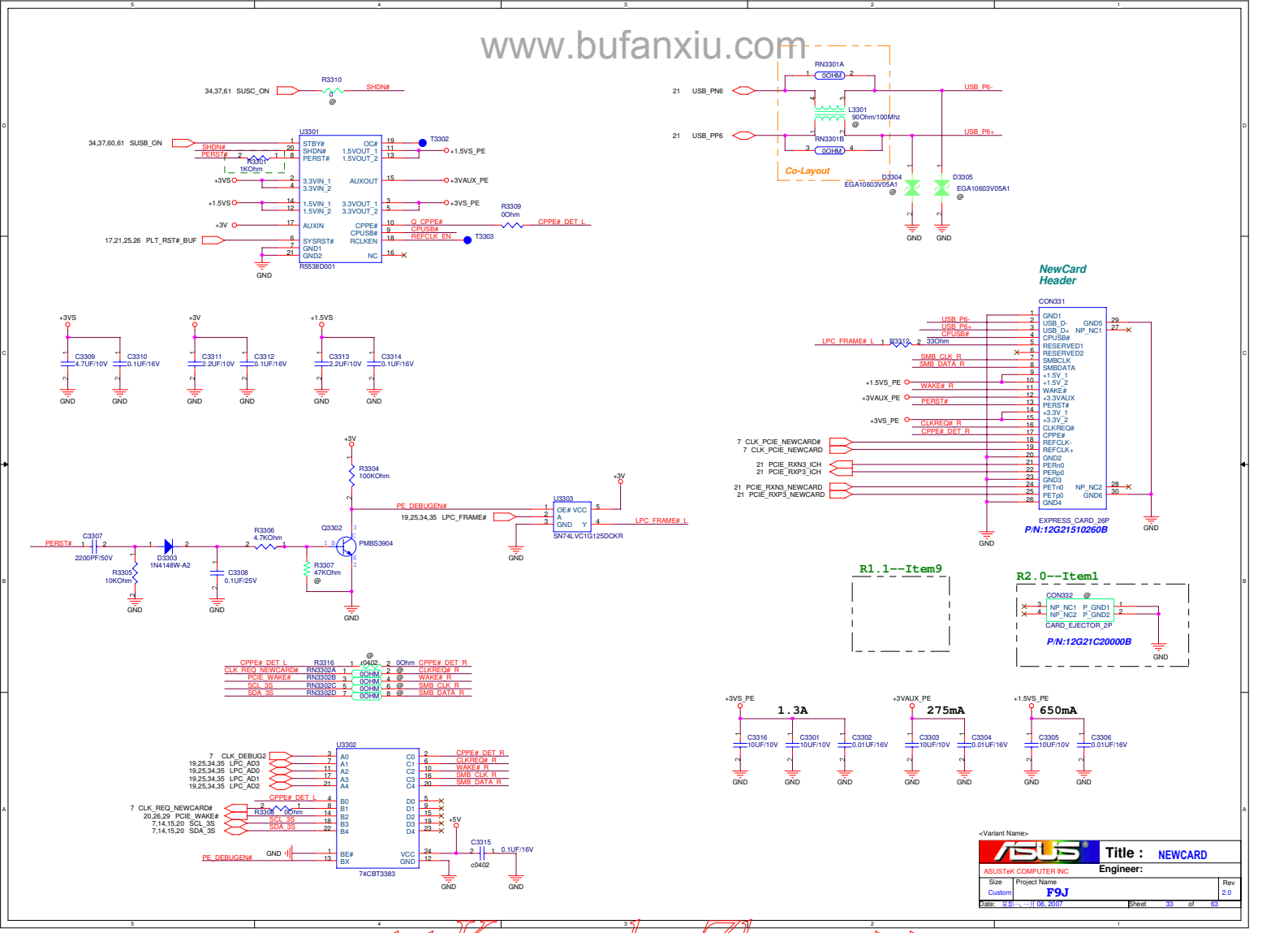
Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

Date: 十月 一, 一日 08, 2007 Sheet 32 of 63



<Variant Name>

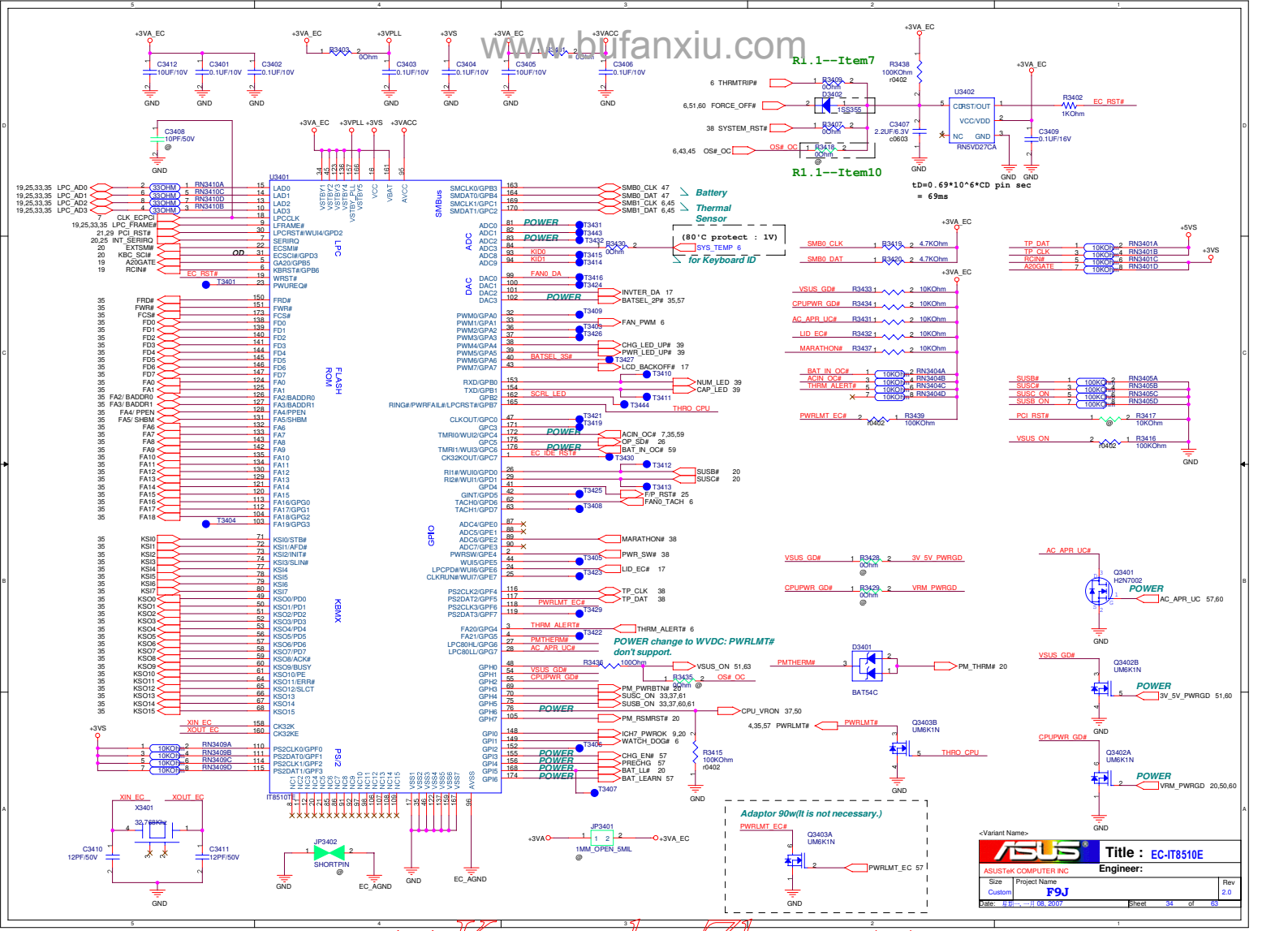
ASUSTeK COMPUTER INC

Title : NEWCARD

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

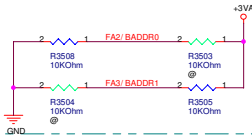
Date: 日 四 一, 一月 08, 2007 Sheet 33 of 63



EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

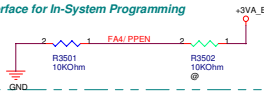
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

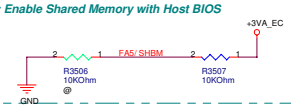
FA4/ PPEN

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

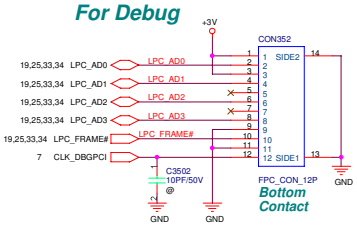


FA5/ SHBM

0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

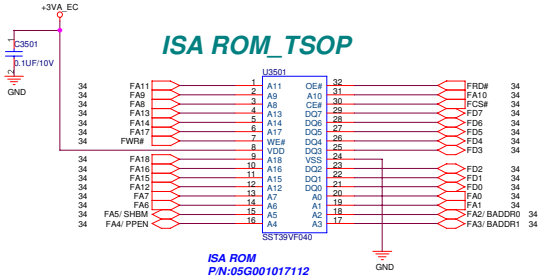


For Debug



Bottom Contact

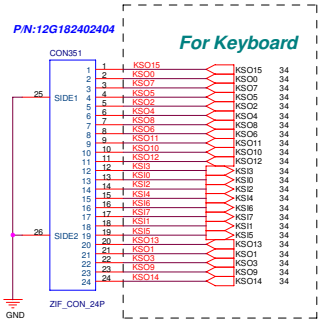
ISA ROM_TSOP

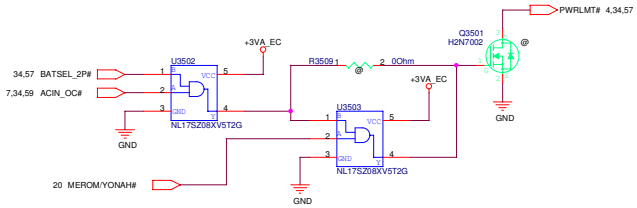


ISA ROM
P/N:05G001017112

P/N:12G182402404

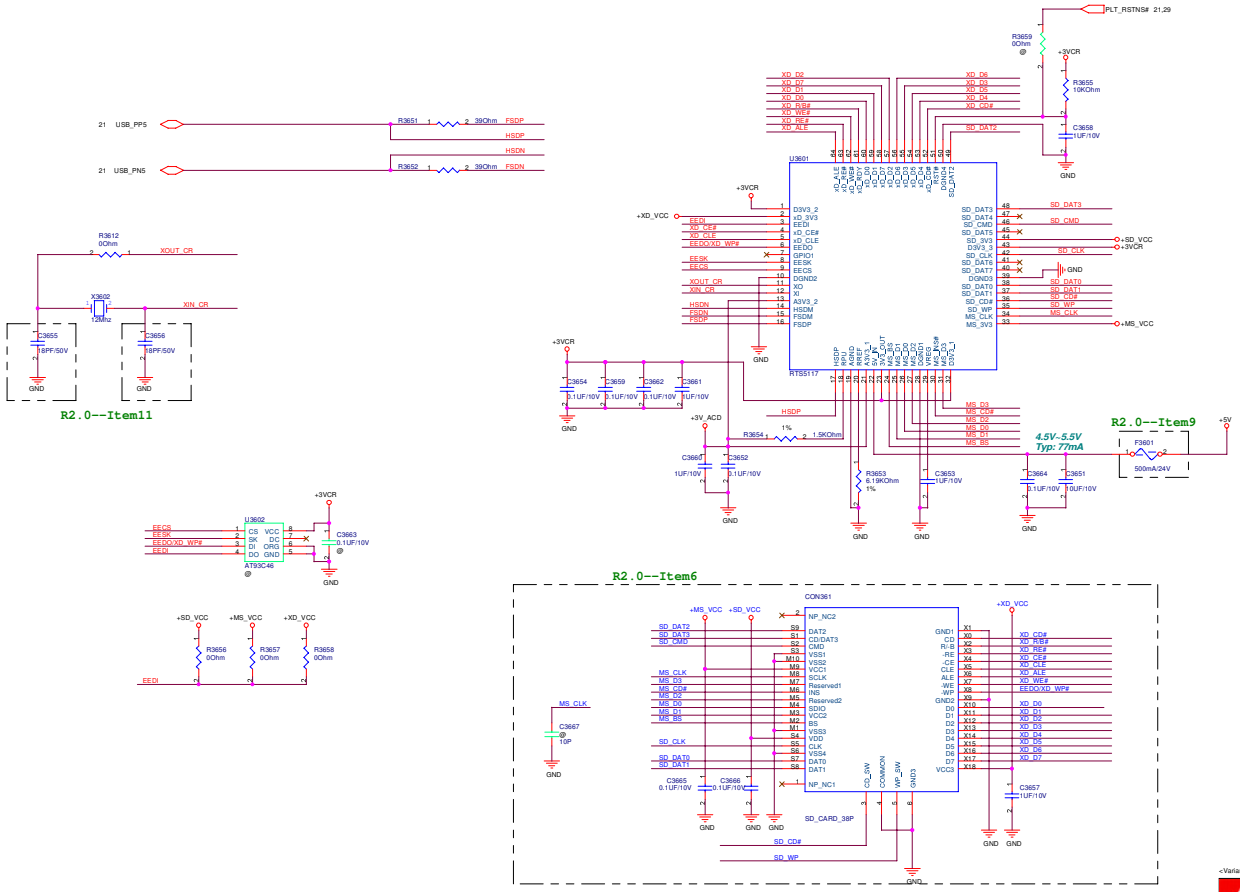
For Keyboard





<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA_ROM&KB conn	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: 年 月 日, 一月 08, 2007	Sheet 35 of 63	



<Variant Name>

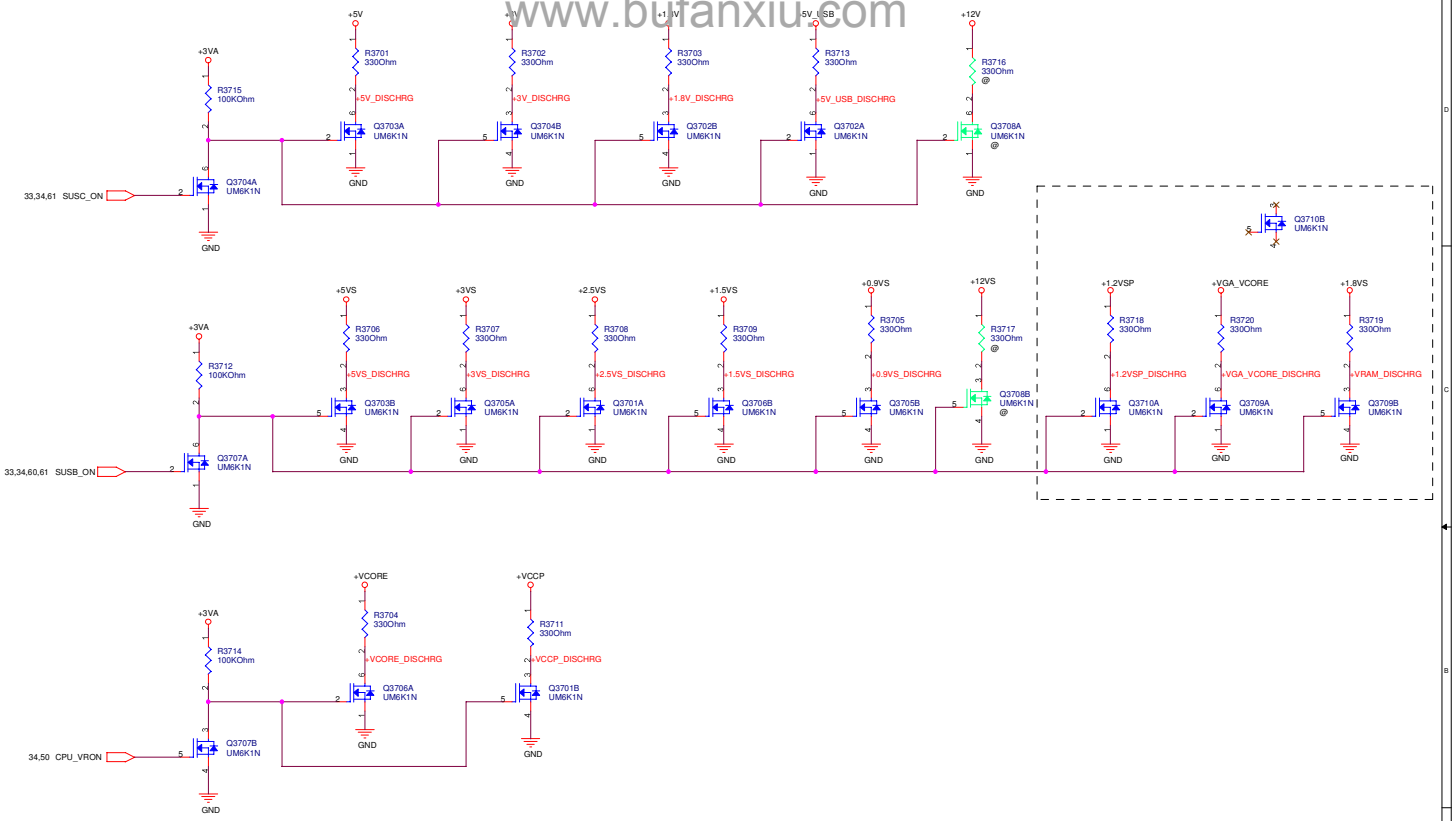
ASUSTeK COMPUTER INC

Title : RTS5117

Engineer:

Size	Project Name	Rev
C	F9J	2.0

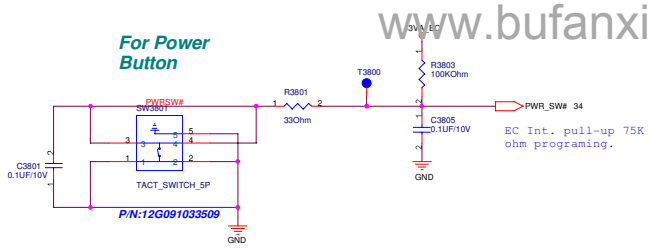
Date: 日 8, 一月 08, 2007 Sheet 38 of 83

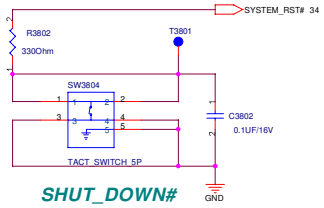


<Variant Name>

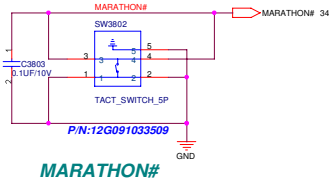
ASUSTeK COMPUTER INC	Title : DISCHARGE	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: 年 08, 2007	Sheet 37 of 63	

For Power Button

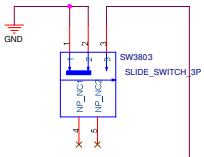




SHUT_DOWN#

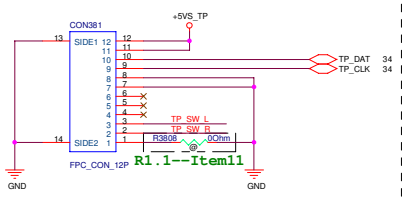


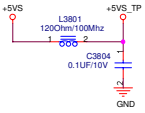
MARATHON#

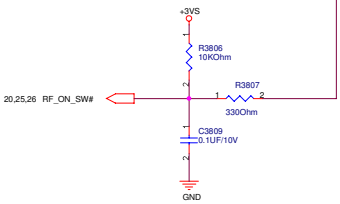


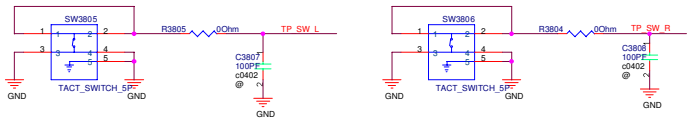
BT/WLAN SW

For Touch-Pad





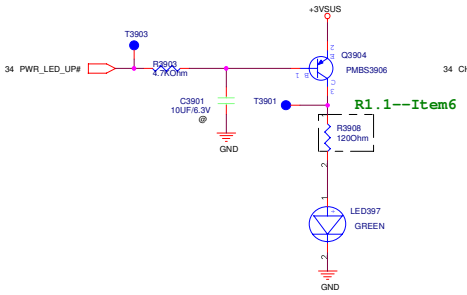




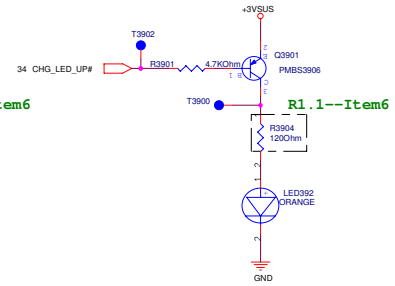
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: 日 8, 2007	Sheet 38 of 63	

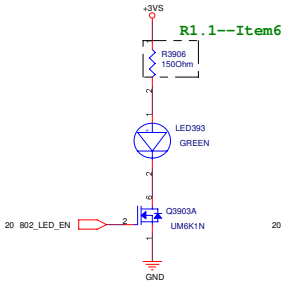
For PWR LED



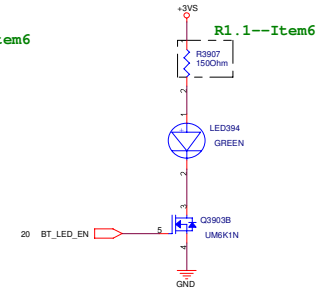
For BATTERY LED



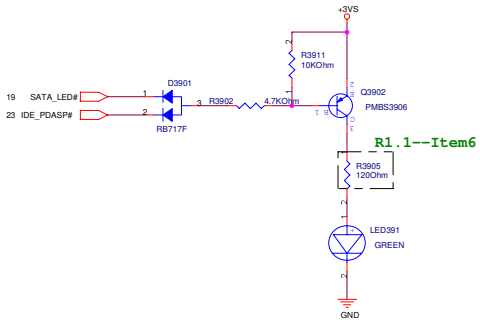
For WireLess LED



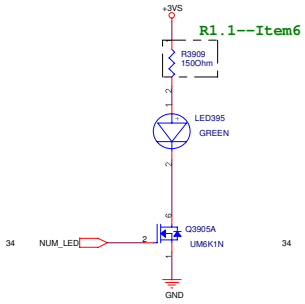
For BT LED



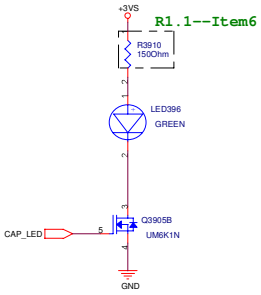
For SATA/IDE LED



For Num Lock

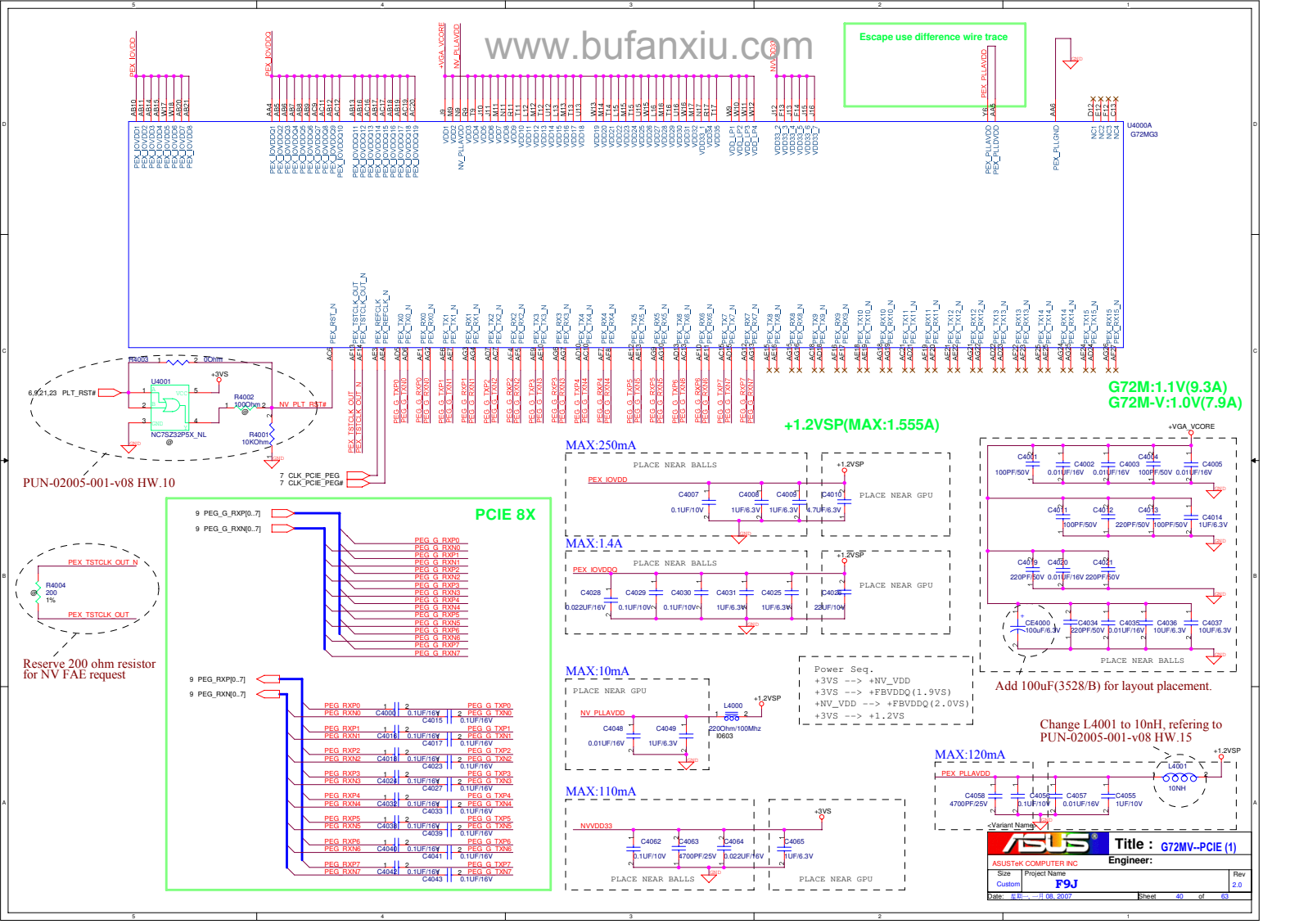


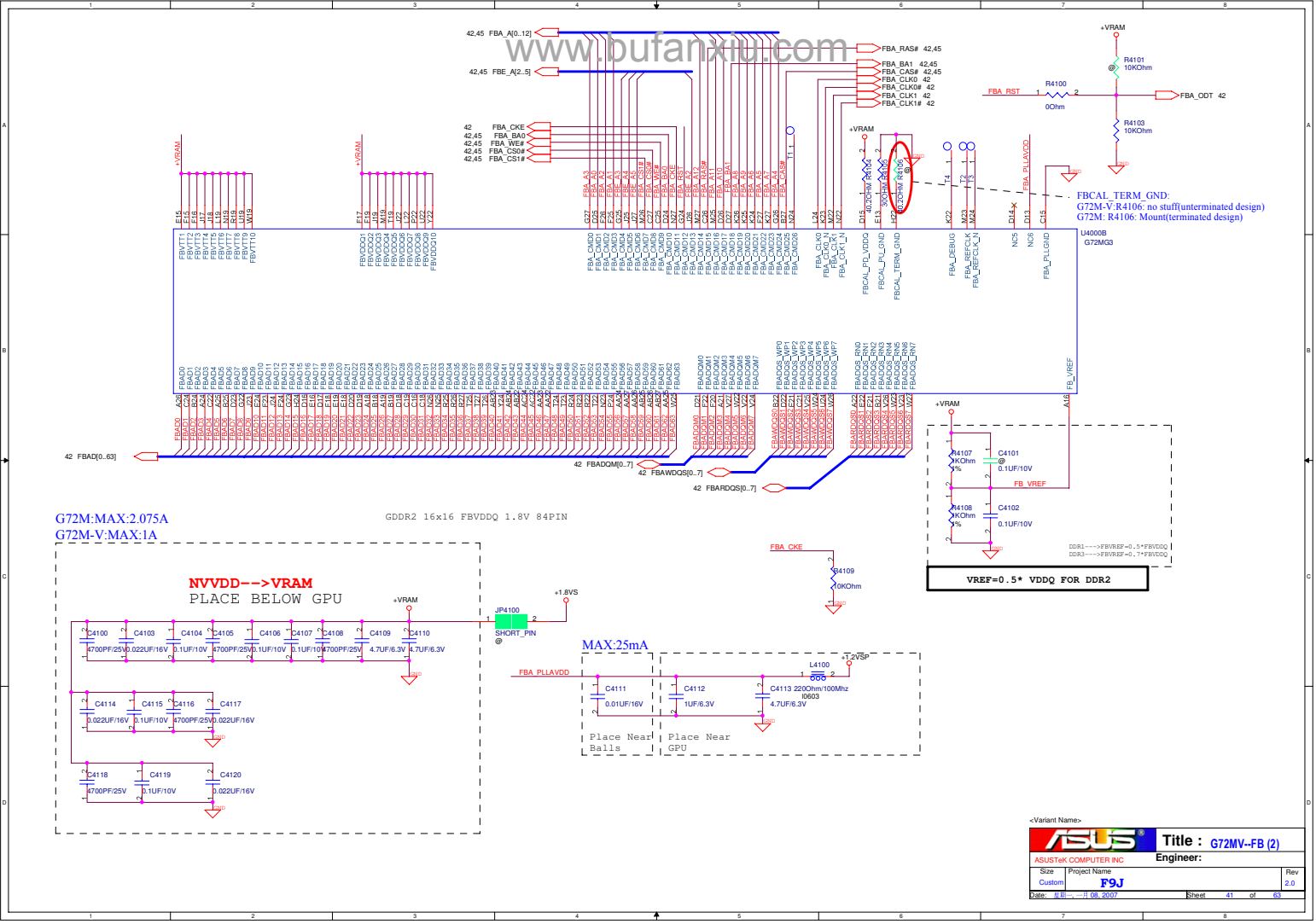
For Cap. Lock



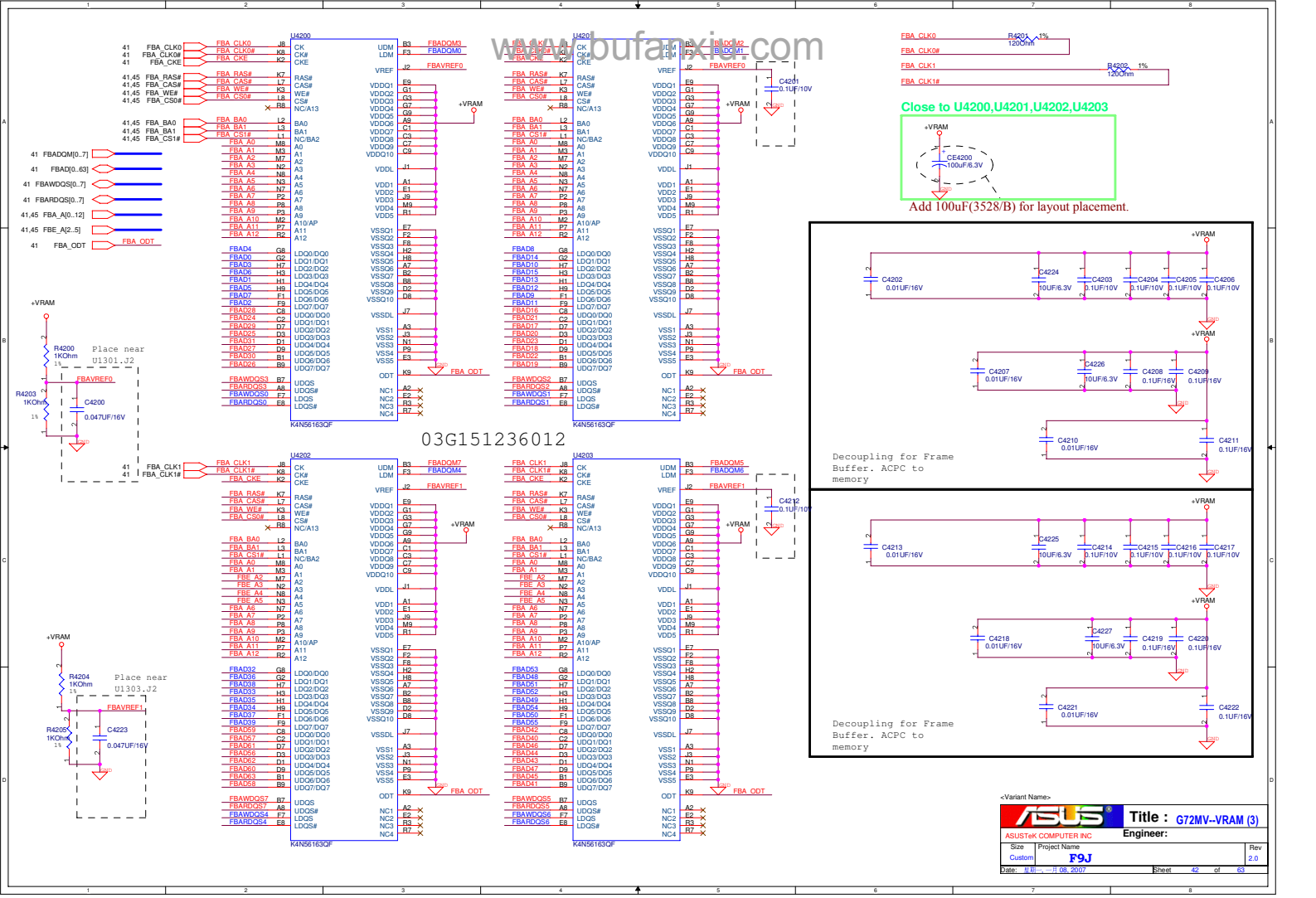
<Variant Name>

ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
Date: 年 月 日, 一	Sheet 39 of 63	





<< Kennedy_Zhang >>



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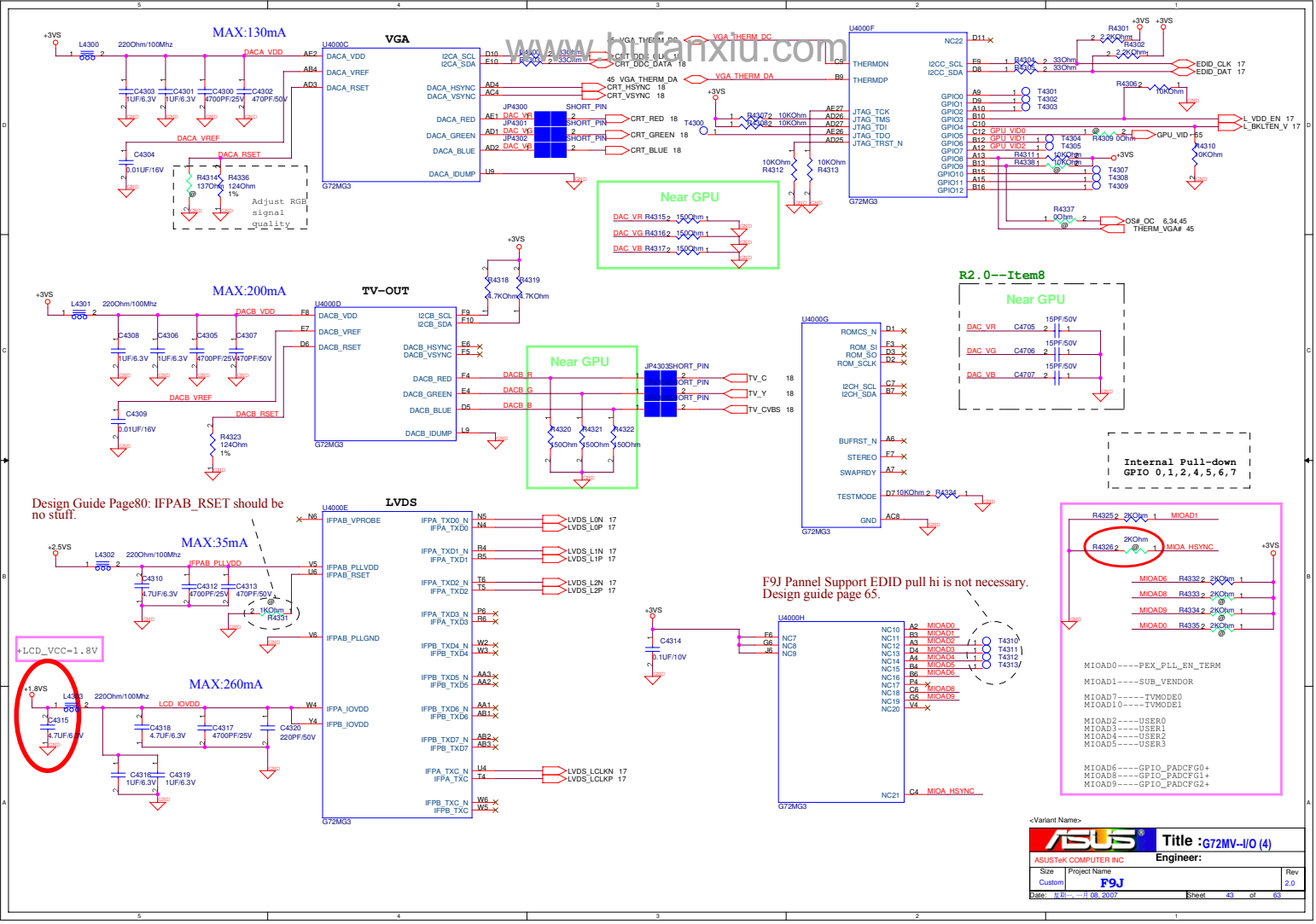
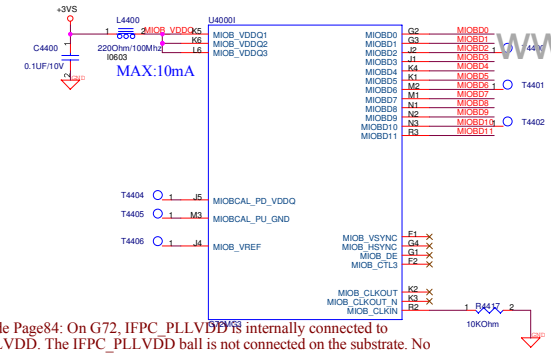
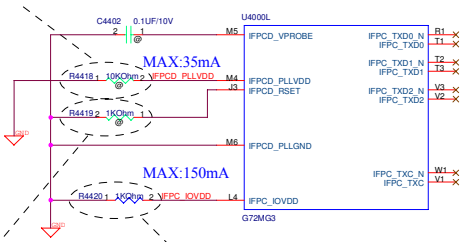


<< Kennedy_Zhang >>

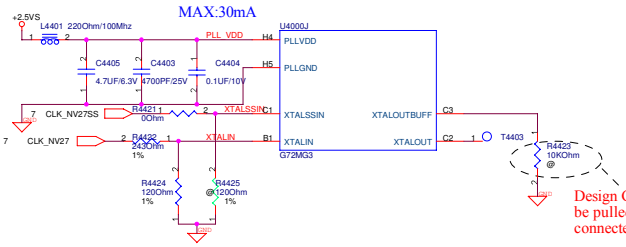


Design Guide Page84: On G72, IFPC_PLLVDD is internally connected to IFPAB_PLLVDD. The IFPC_PLLVDD ball is not connected on the substrate. No connection or filter is required.(V6,W7J:Mount 10Kohm)



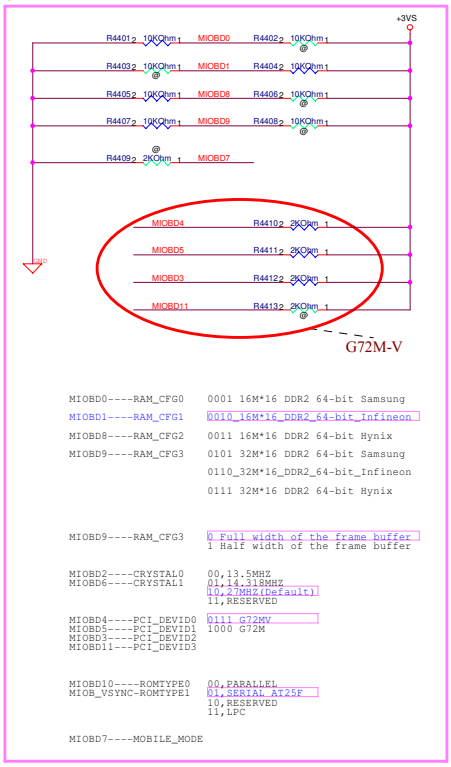
Design Guide Page80:
IFPCD_RSET should
be no stuff.(V6,W7J:no stuff)

Design Guide Page84: Suggest pull low 1K ohm(V6,W7J:10Kohm)

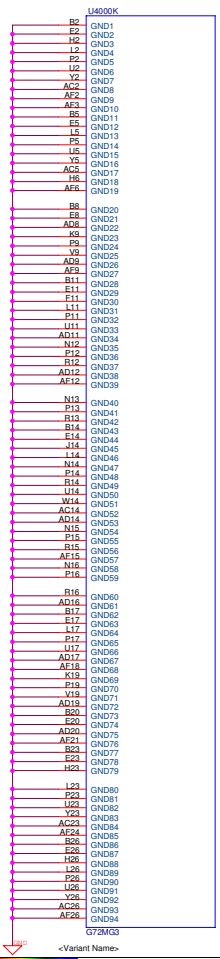


Design Guide Page63: The XTALOUTBUF signal should be pulled down using a 60 Ω resistor if it is not connected to an external device. (Check NV FAE)

STRAP




```
MIOBD0----RAM_CFG0     0001 16M*16 DDR2 64-bit Samsung
MIOBD1----RAM_CFG1     0010_16M*16_DDR2_64-bit_Infineon
MIOBD8----RAM_CFG2     0011 16M*16 DDR2 64-bit Hynix
MIOBD9----RAM_CFG3     0101 32M*16 DDR2 64-bit Samsung
                       0110_32M*16_DDR2_64-bit_Infineon
                       0111 32M*16 DDR2 64-bit Hynix

MIOBD9----RAM_CFG3     0 Full width of the frame buffer
                       1 Half width of the frame buffer

MIOBD2----CRYSTAL0     00,13.5MHZ
MIOBD6----CRYSTAL1     01,14.318MHZ
                       10,27MHZ(Default)
                       11,RESERVED

MIOBD4----PCI_DEVID0   0111 G72MV
MIOBD5----PCI_DEVID1   1000 G72M
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3

MIOBD10----ROMTYPE0    00,PARALLEL
MIOB_VSYNC-ROMTYPE1    01,SERIAL AT25F
                       10,RESERVED
                       11,LPC

MIOBD7----MOBILE_MODE
```



ASUSTeK COMPUTER INC	Title : G72MV--TMDS (5)	
	Engineer:	
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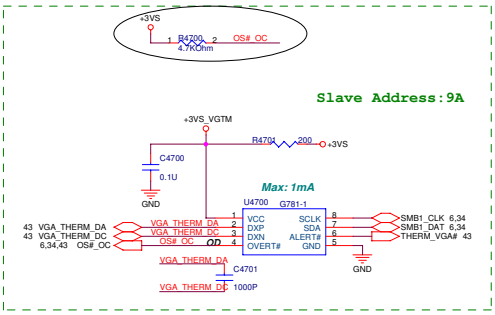
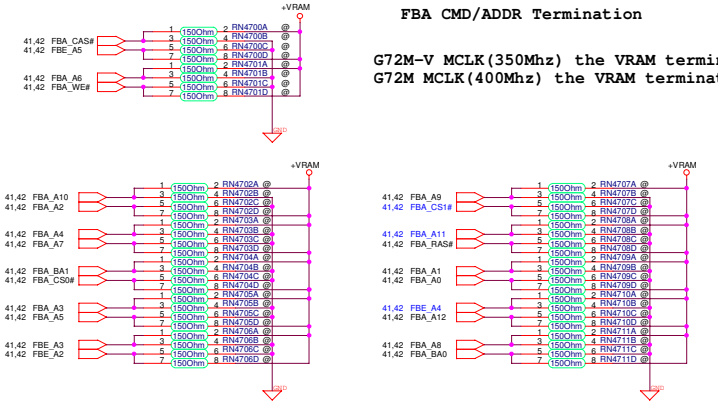
<< Kennedy_Zhang >>

OS#_OC connector to EC U3402(pin5) Dnl R4700



FBA CMD/ADDR Termination

G72M-V MCLK(350Mhz) the VRAM termination is not necessary.
G72M MCLK(400Mhz) the VRAM termination is necessary.



CMD/ADDR termination resistors 150ohm. Design Guide Page47

<Variant Name>

ASUSTeK COMPUTER INC

Title G72MV--VRAM_TERM

Engineer:

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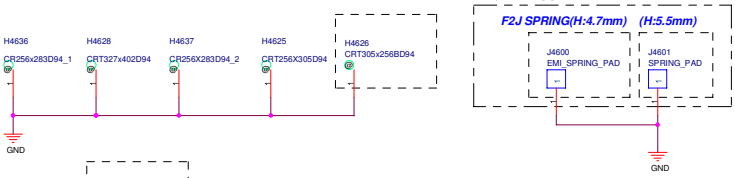
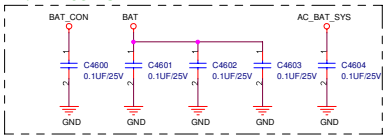
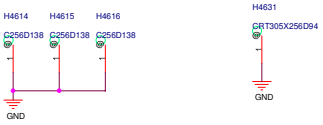
R1.1--Item12 EMI SPRING

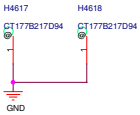
F2J SPRING(H:4.7mm) (H:5.5mm)

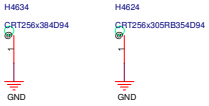


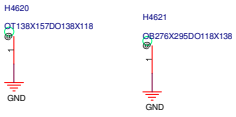
R1.1--Item13











<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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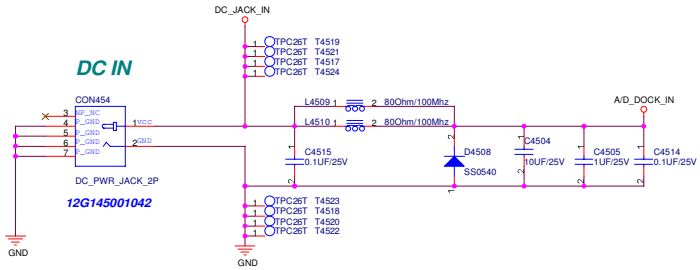
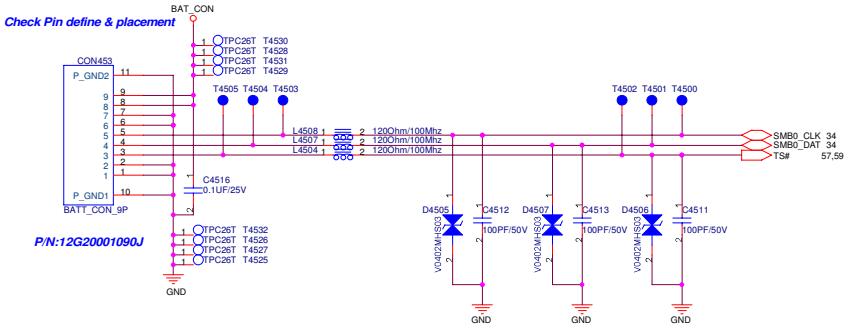
DC IN



BAT IN

Check Pin define & placement



<Variant Name>

ASUSTeK COMPUTER INC

Title : G72M-Terminator

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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F9J SR_0928(R1.0---->R1.1)

(1)Change the s-vedio CON(CON182) to 12G14101107K for SMT issue.---page18.

(2)R1707 change from 10Kohm to 100Kohm to solve the LCD flash during warm boot.---Page17

(3)CON361(4 in 1) change to 12G340003800 to solve the factory yield rate issue.---Page36

(4)Add R2309 and R2310 for IDE select---Page 23

(5)Add C2512(10UF/10V) for FP power---Page 25

(6)Change R3904,R3905 and R3908 to 120 ohm, change R3906,R3907,R3909 and R2910 to 150 ohm to control LED current is about 10mA.---Page 39

(7)Del R3418, R3408,R617 and Q605,and add D3402 and D3403 for the OS#_OC function.---Page6; Page 34

(8)Reserved R2038 10K for GPIO10 pull high and R2039 10K for GPIO25 pull high.---Page 20

(9)Add NPTH H3301 & H3302 for New Card EJECTOR CON for ME request.---Page33

(10)Modify OS#_OC schematic: add R617 ; Q605 & reserved R3418.---Page6; Page34.

(11)Reserved R3808 0 ohm to support ALPS TP.---Page38

(12)Add J4600;J4601 EMI SPRING for EMI request.---Page46

(13)Change C2510 from 0.1u to 1uF for FP power.---Page25

(14)Reserved Change Cap C4600-C4604(0.1uF) for ESD issue of Buttom floating part ---Page46

(15)Mount voltage protector on D2503 for ESD issue of Finger printer.---Page25

(16)Mount 10uF capacitor on C534,C538,C533,C535,C536.---Page5

(17)Mount 600 ohm Bead on L1814,L1815,L1816 and 100P capacitor on C1839 ~C1844 for EMI issue of S-terminal.---Page18
(ER double check signal quality).

F9J ER_1102(R1.1---->R2.0)

(1) Update new CARD_EJECTOR_2P(CON332) footprint(add 2 npth hole) & remove 2 npth hole(H3301;H3302).---Page33

(2) Change the ODD CON(CON232) from 12G16121050P to 12G161240501 for ME request.(Board lock hole:1.8mm; 3.0H)---Page23

(3) Change the TV filter circuit. (Follow G72M design guide); this circuit can pass TV signal quality & EMI testing.---Page18

(4) Change R1816 & R1817 from 0ohm to 33ohm; mount cap 22pf on C1837 & C1838 for VSYNC/HSYNC.---Page18

(5) R753 & R755 change from 33ohm to 0ohm for CLK_PCIE_MINICARD#/CLK_PCIE_MINICARD signal quality.---Page7

(6)CON361 change from 12G340003800 to 12G340003810 to improve the yield rate.---Page36

(7)Add test point for factory request:
T1910(+RTCBAT);D1901 PIN2(T1911);+5V_USB(T2400);BAT_LL#(T3407);PWRSW#(R3801_2)(T3800);CHG_LED_UP(Q3901_3)(T3900);PWR_LED_UP(Q3904_3)(T3901).

(8)For CRT signal quality & EMI issue change the filter components:
a.L1811-L1813 change to 0.082uH
b.C1831;C1833;C1835 change from 15pF to 22pF.
c.C1832;C1834:C1836 change from 22pF to 2pF.
d.Add C4705;C4706;C4707 15pF.

(9)Change the card reader fuse(F3601) from 0.2A/30V to 0.5A/24V.(250mA_flash card + 77mA _ core logic)

(10)R1806,R1807 change to L1806;L1807(120 ohm bead) to improve the noise from CRT port for EMI request.

(11)C3658/C3655 change from 15pF to 18pF for card reader crystal adjustment.

(12)CCD polyswitch(F1701) change to 07G014050102(RAYCHEM 500mA).

(13)R1705 change from 100ohm to 390 ohm to meet CMO discharge timming(8ms)(spec >5ms).

F9J ER_0104(R2.00---->R2.01)

(1)Change CON331 to 12G21510260B NEW CARD HEADER 26P 3H
REV TAITWUN/PXPWDE-000LBS2ZZ4N0---Page33

<Variant Name>

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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<Variant Name>

Title : History(2)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9J	2.0

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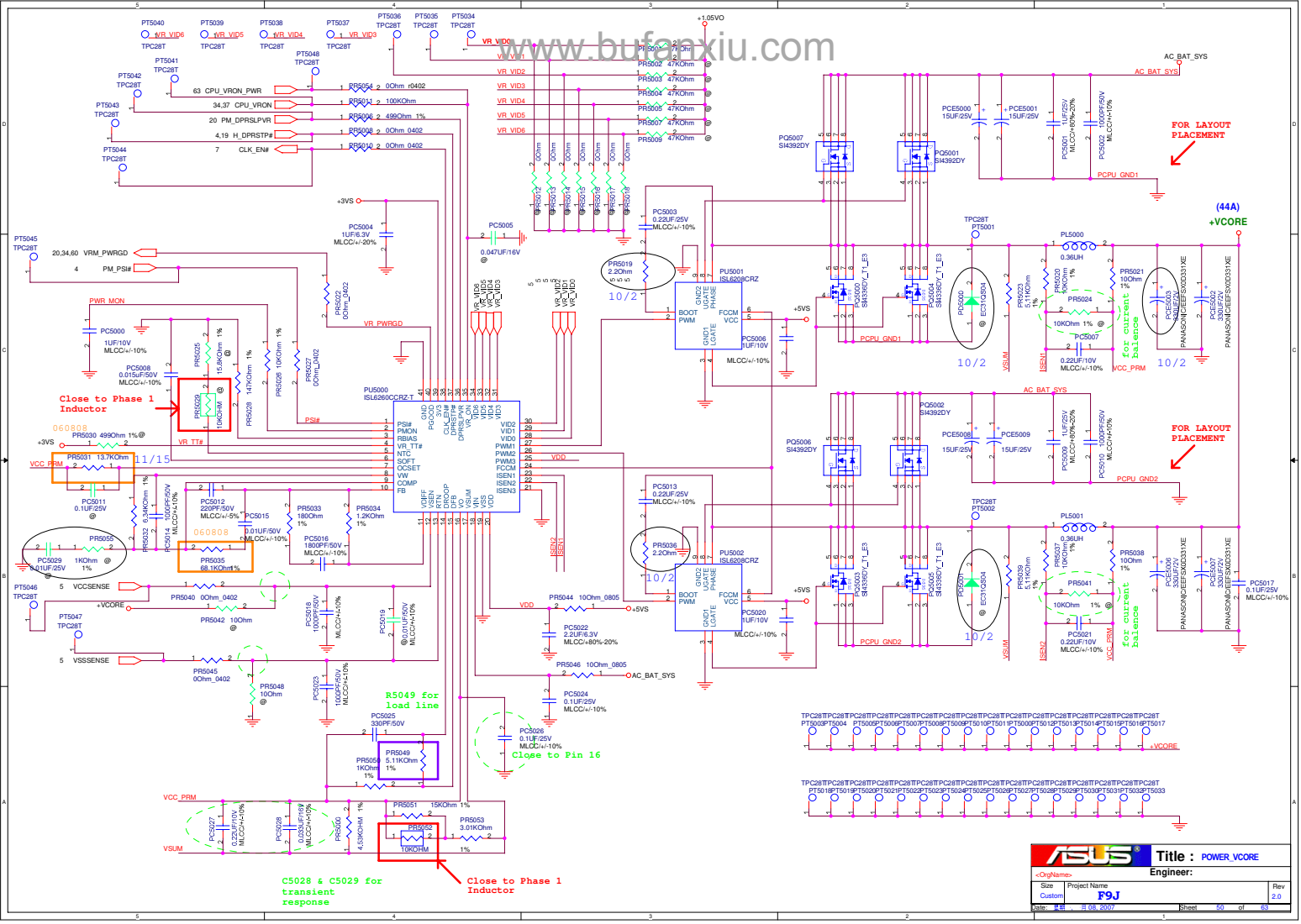
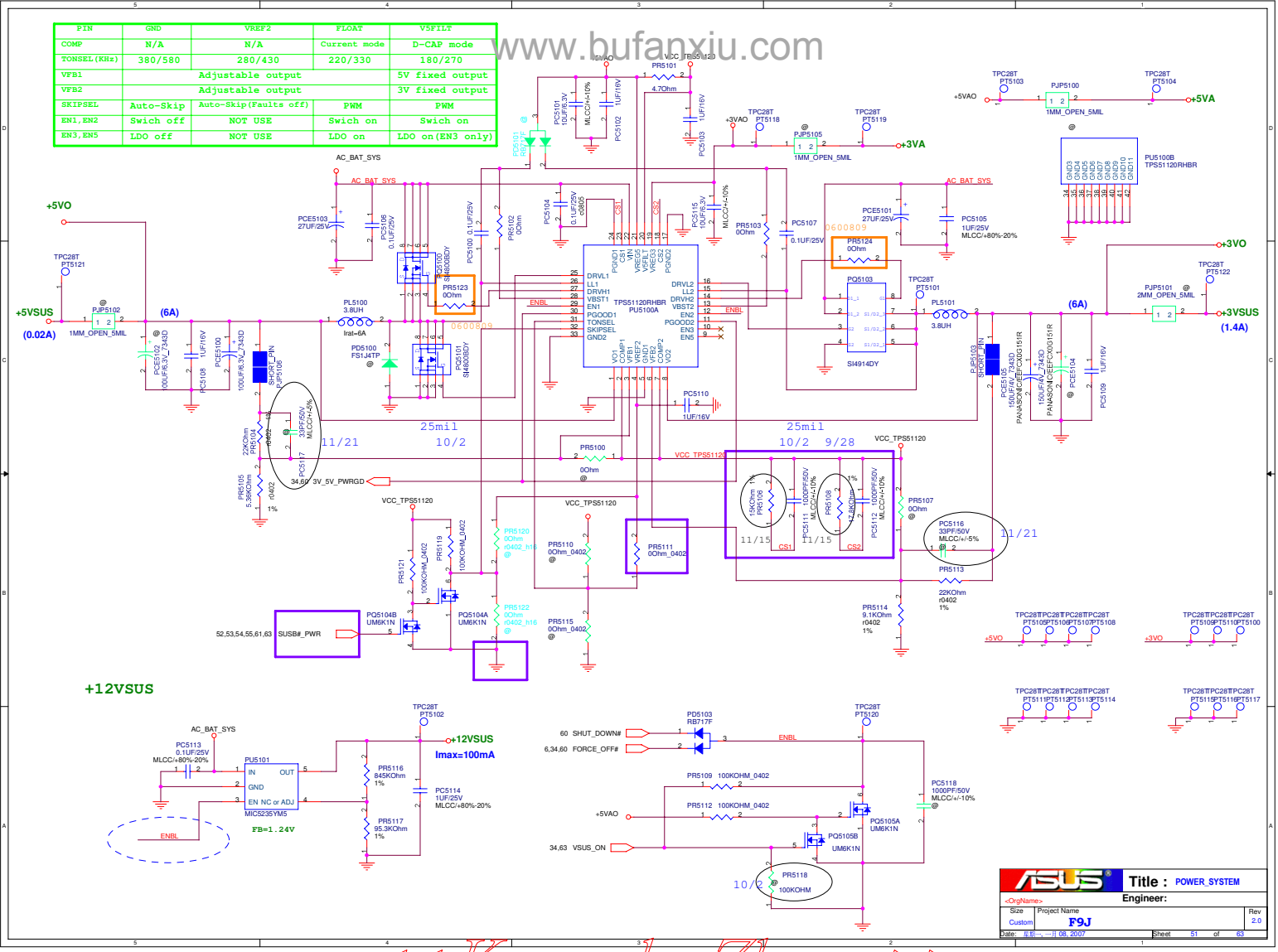


<< Kennedy_Zhang >>

PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output			5V fixed output
VFB2	Adjustable output			3V fixed output
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)



Title : POWER_SYSTEM				
<OrgName>	Engineer:			
Size: Custom	Project Name: F9J			Rev: 2.0
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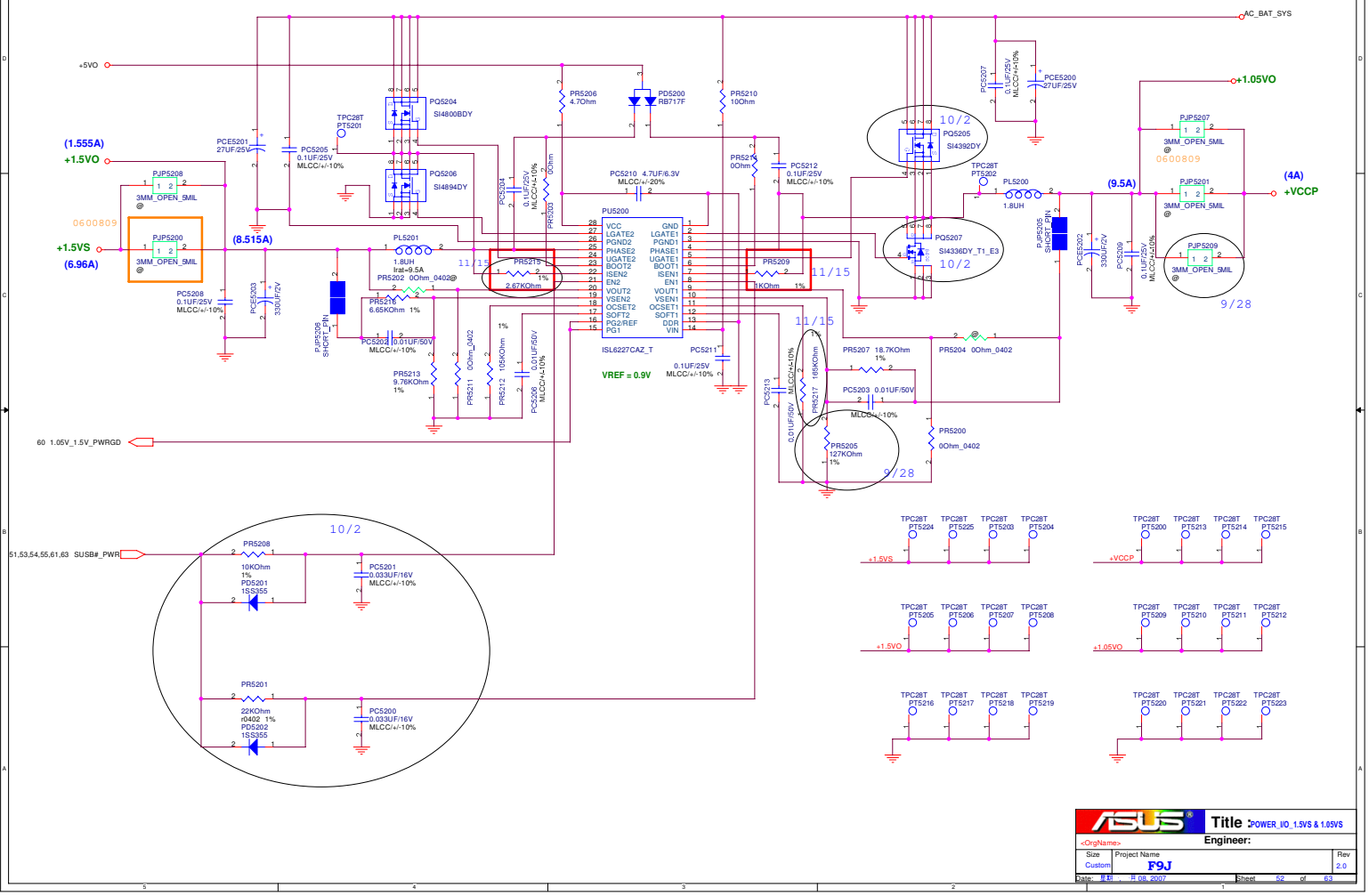
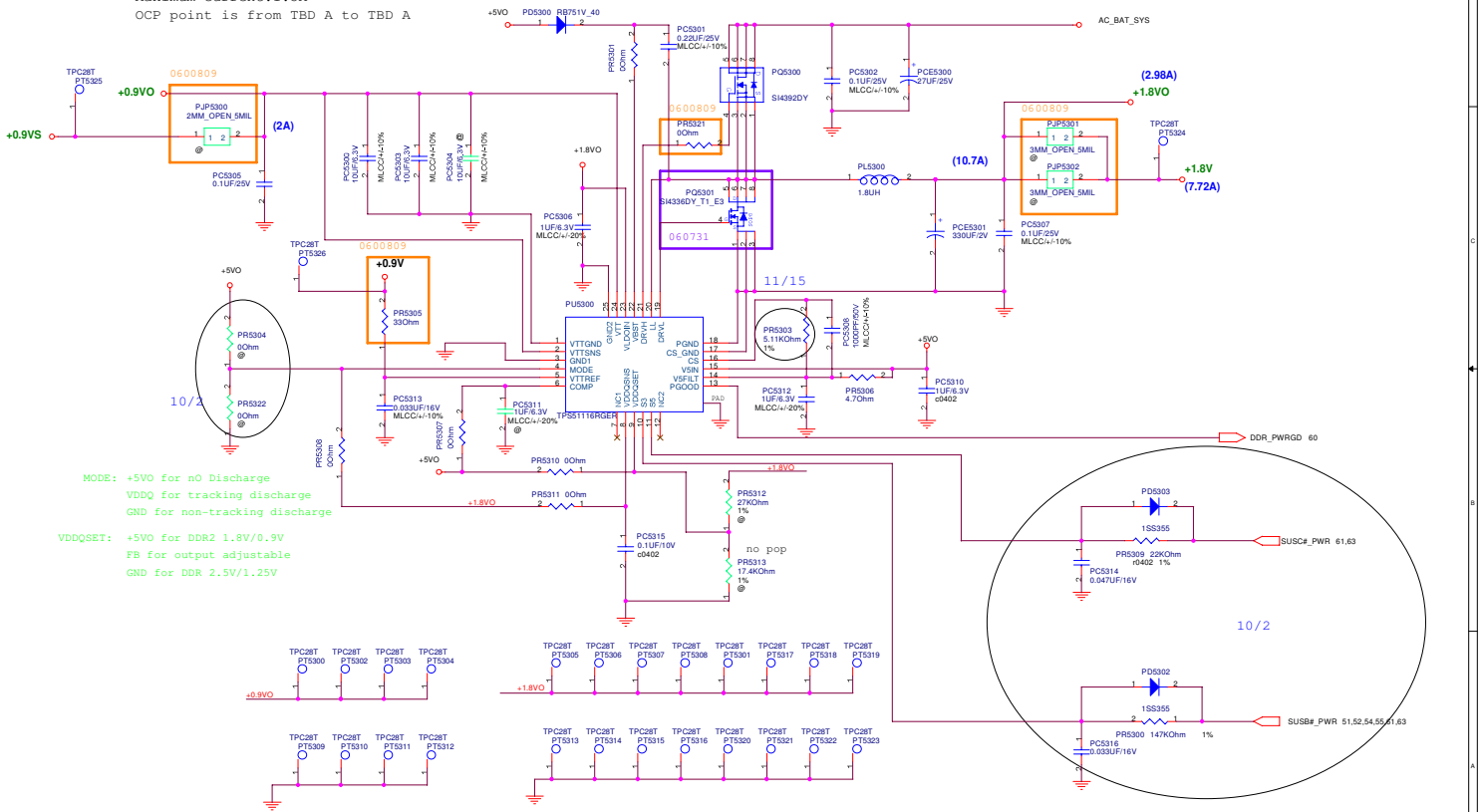


<< Kennedy_Zhang >>

.9 Volt +/-5%.9 Volt +/-5%
Design Current:1.05A
Maximum current:1.5A
OCP point is from TBD A to TBD A

1.8Volt +/-5%
Design Current:7.3A
Maximum current:10.5A
OCP point is from TBD A to TBD A



ASUS

Title : POWER_I/O_DDR & VTT

<OrgName>

Engineer:

Size	Project Name	Rev
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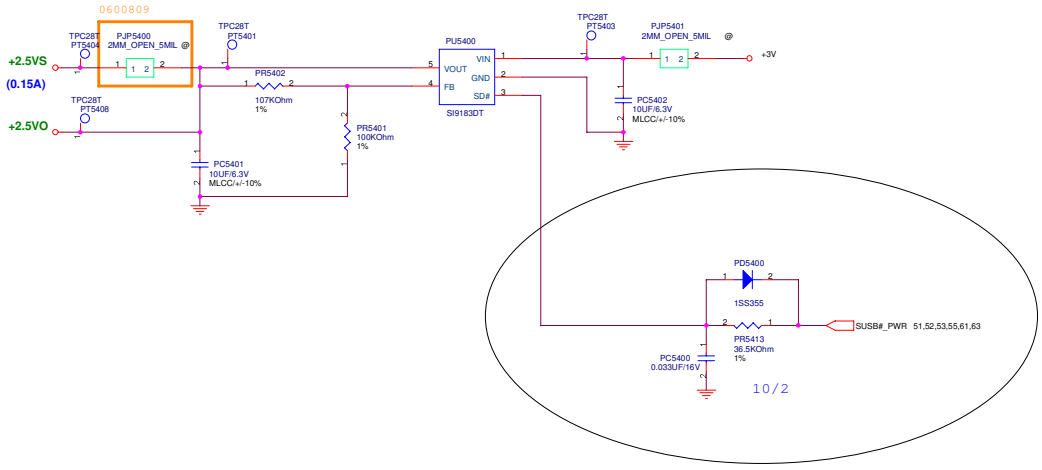
<< Kennedy_Zhang >>

+2.5VS



Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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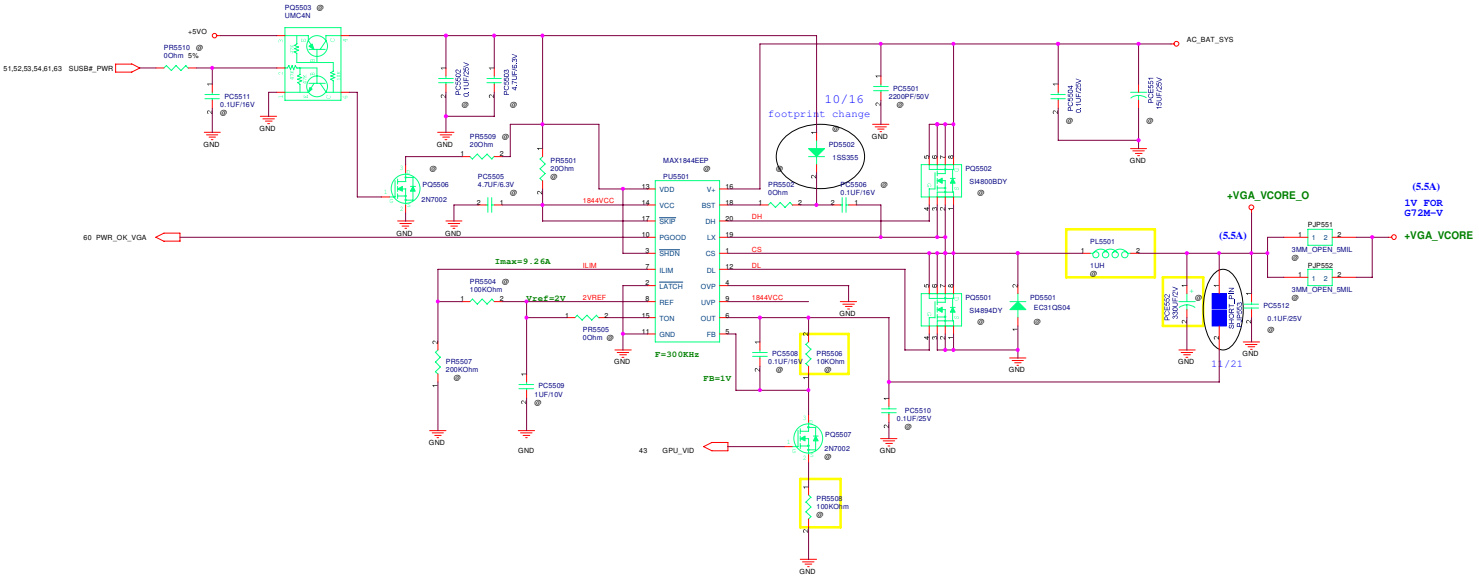

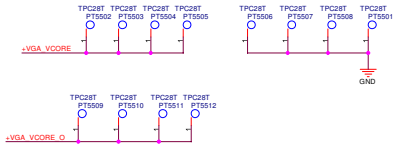

Title : POWER_VGA_VCORE			
<Org.Name>	Engineer:		
Size: Custom	Project Name: F9J		Rev: 2.0
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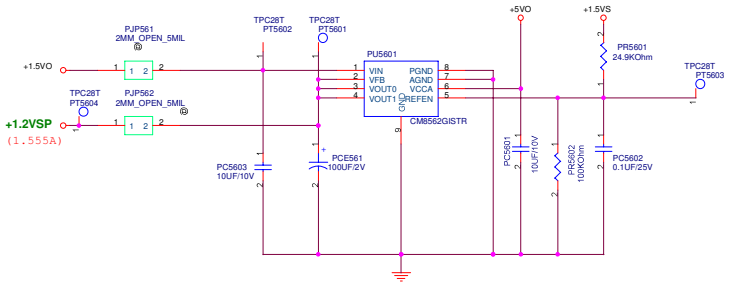

ASUS	Title : +1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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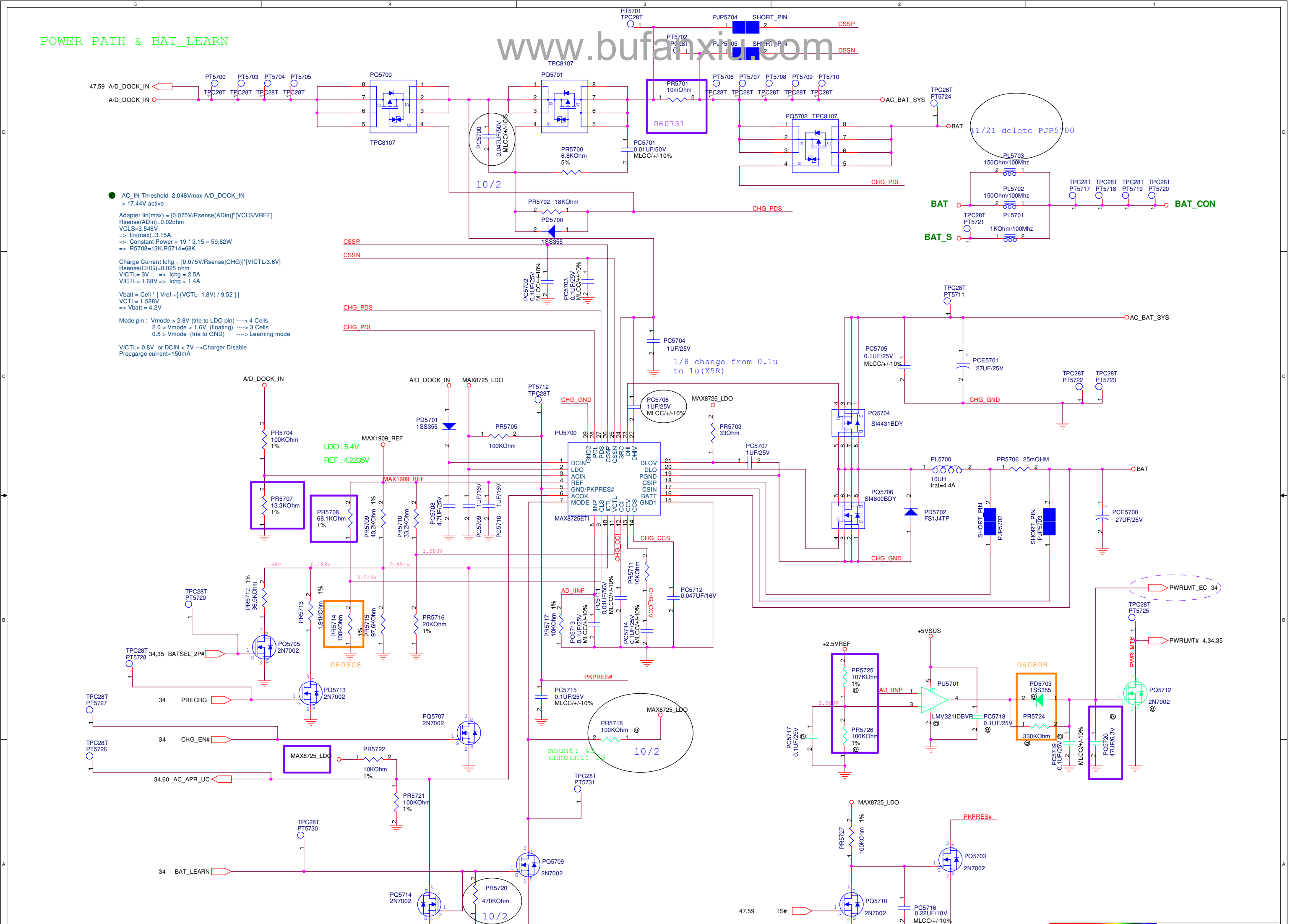

POWER PATH & BAT_LEARN
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02ohm
VCLS=3.546V
=> Iin(max)=3.15A
=> Constant Power = 19 * 3.15 = 59.82W
=> R5708=13K,R5714=68K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ---> 4 Cells
2.0 > Vmode > 1.6V (floating) ---> 3 Cells
0.8 > Vmode (trie to GND) ---> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
A/D_DOCK_IN
AC_BAT_SYS
BAT
BAT_CON
BAT_S
11/21 delete PJP5700
060731
10/2
1/8 change from 0.1u to 1u(X5R)
LDO : 5.4V
REF : 4.2235V
060808
MAX8725ETI
PU5700
PU5701 LMV321IDBVR
CSSP
CSSN
CHG_PDS
CHG_PDL
CHG_GND
CHG_CCS
PKPRES#
AD_IINP
MAX8725_LDO
MAX1909_REF
BATSEL_2P#
PRECHG
CHG_EN#
AC_APR_UC
BAT_LEARN
TS#
PWRLMT_EC
PWRLMT#
+2.5VREF
+5VSUS

Title : POWER_CHARGER

Engineer:

<OrgName>

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Title : POWER_PIC			
<OrgName>	Engineer:		
Size: Custom	Project Name: F9J		Rev: 2.0
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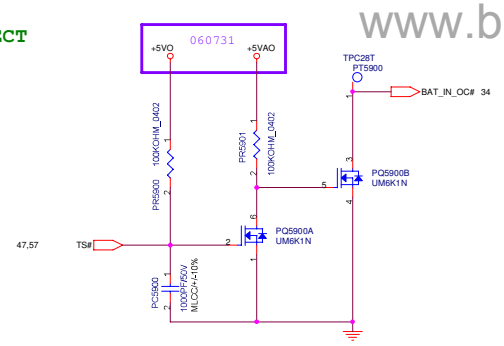
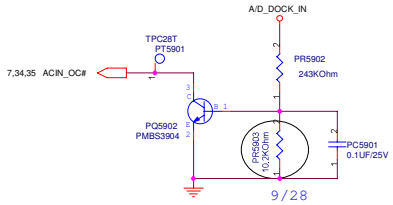
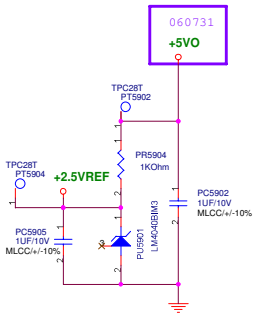
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
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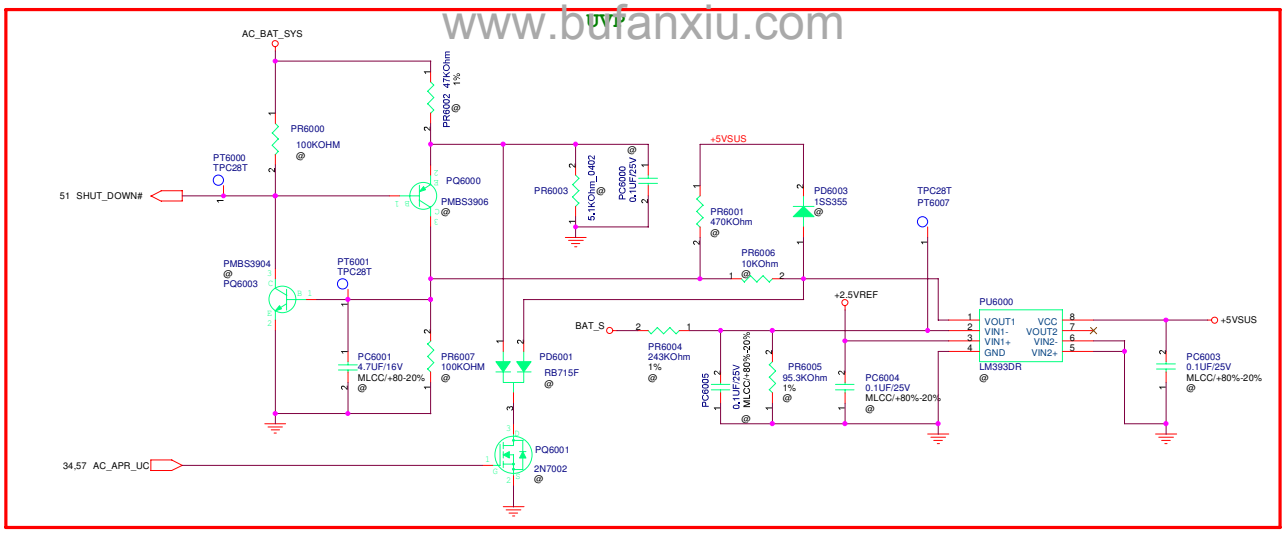
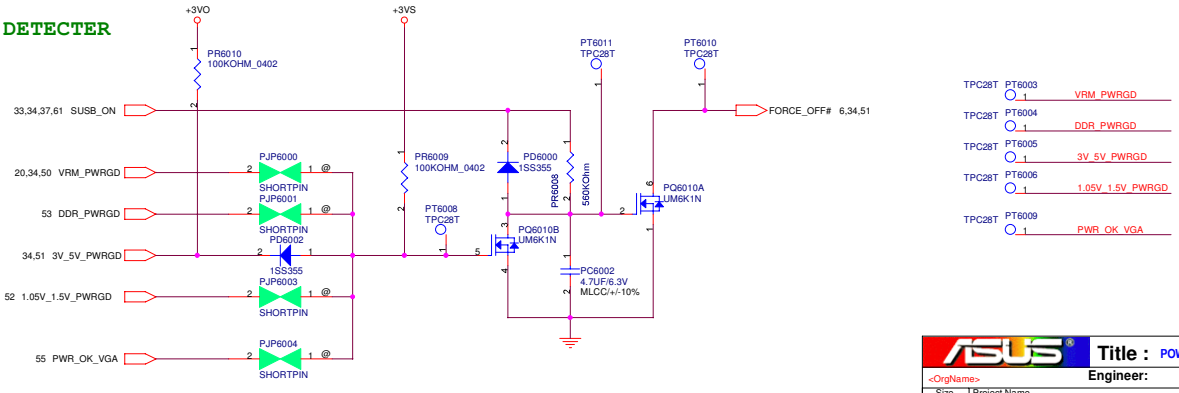


POWER GOOD DETECTER



ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F9J	Rev: 2.0
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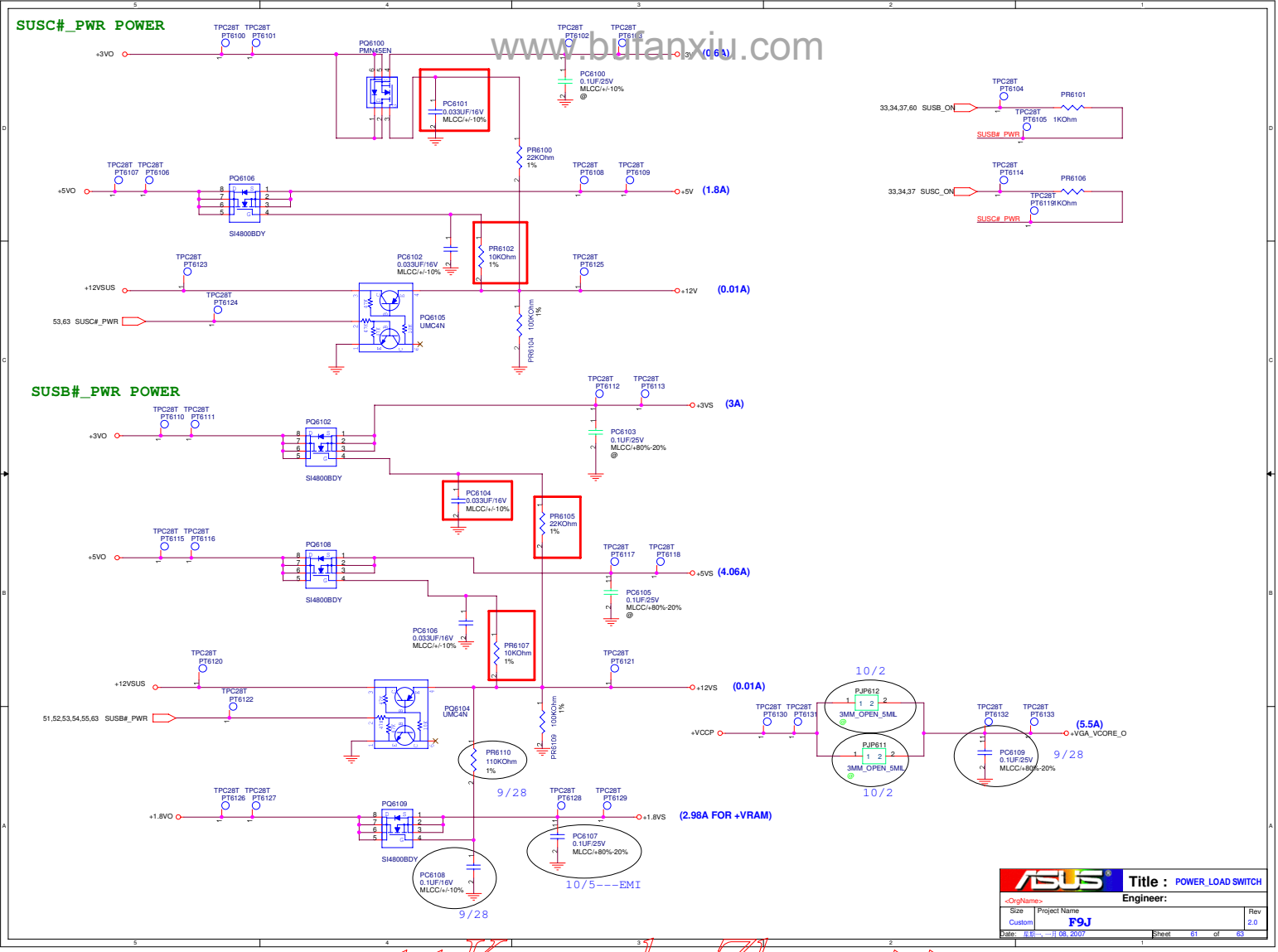


AC_BAT_SYS → AC_BAT_SYS 17,50,51,52,53,55,57,60
+3VA → +3VA 17,19,34,37,51
+5VA → +5VA 51
+5VO → +5VO 51,52,53,55,56,59,61
+3VO → +3VO 51,60,61
+3VSUS → +3VSUS 17,20,21,22,26,29,39,51
+5VSUS → +5VSUS 22,51,57,60
+3V → +3V 21,25,26,33,35,37,54,61
+3VS → +3VS 6,7,9,11,13,14,15,17,18,20,22,23,25,26,29,33,34,37,38,39,40,43,44,45,50,60,61

+12VSUS → +12VSUS 51,61
+12V → +12V 24,26,37,61
+12VS → +12VS 17,37,61

+5V → +5V 17,24,33,36,37,61
+5VS → +5VS 6,18,22,23,25,26,34,37,38,50,61

+2.5VO → +2.5VO 54
+2.5VS → +2.5VS 11,37,43,44,54
+1.8VO → +1.8VO 53,61
+1.8V → +1.8V 9,12,14,15,37,53

+VCCP → +VCCP 5,12,22,37,52,61

+0.9VS → +0.9VS 16,37,53
BAT → BAT 57

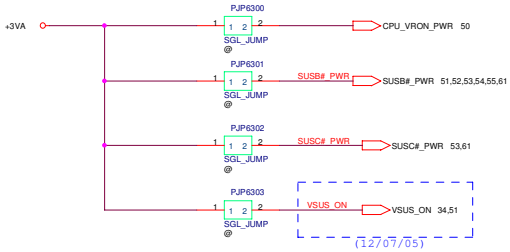
+2.5VREF → +2.5VREF 57,59,60
+VCORE → +VCORE 5,37,50

BAT_CON → BAT_CON 47,57

+1.2VSP → +1.2VSP 37,40,41,56

+VGA_VCORE → +VGA_VCORE 37,40,55

FOR POWER TEST



Title : POWER_SIGNAL		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F9J	Rev: 2.0
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